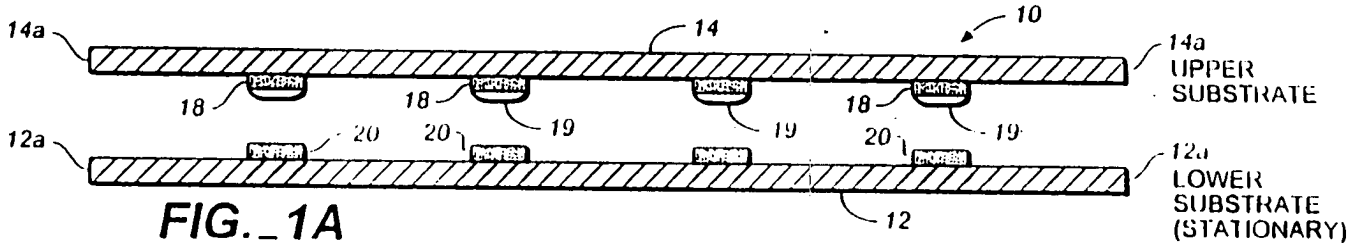


FIG._1A

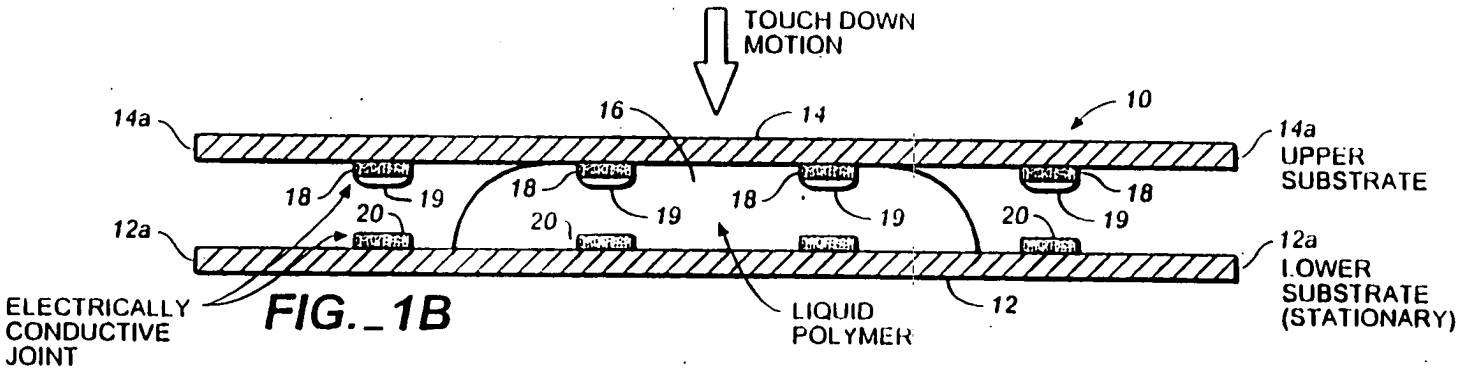


FIG._1B

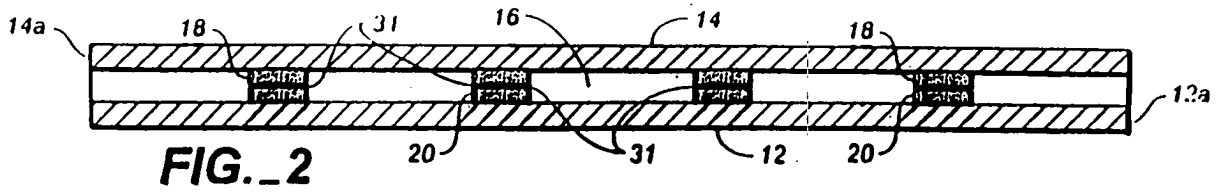


FIG._2

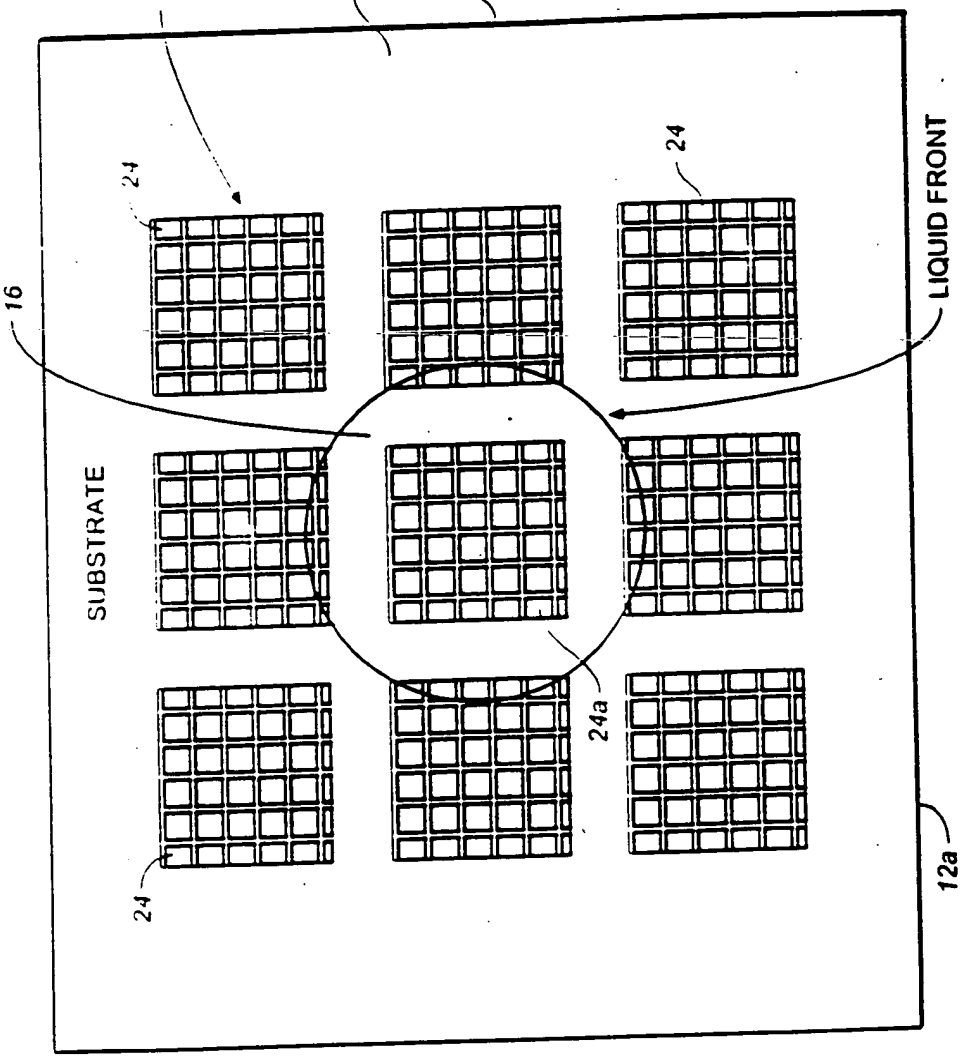


FIG._3

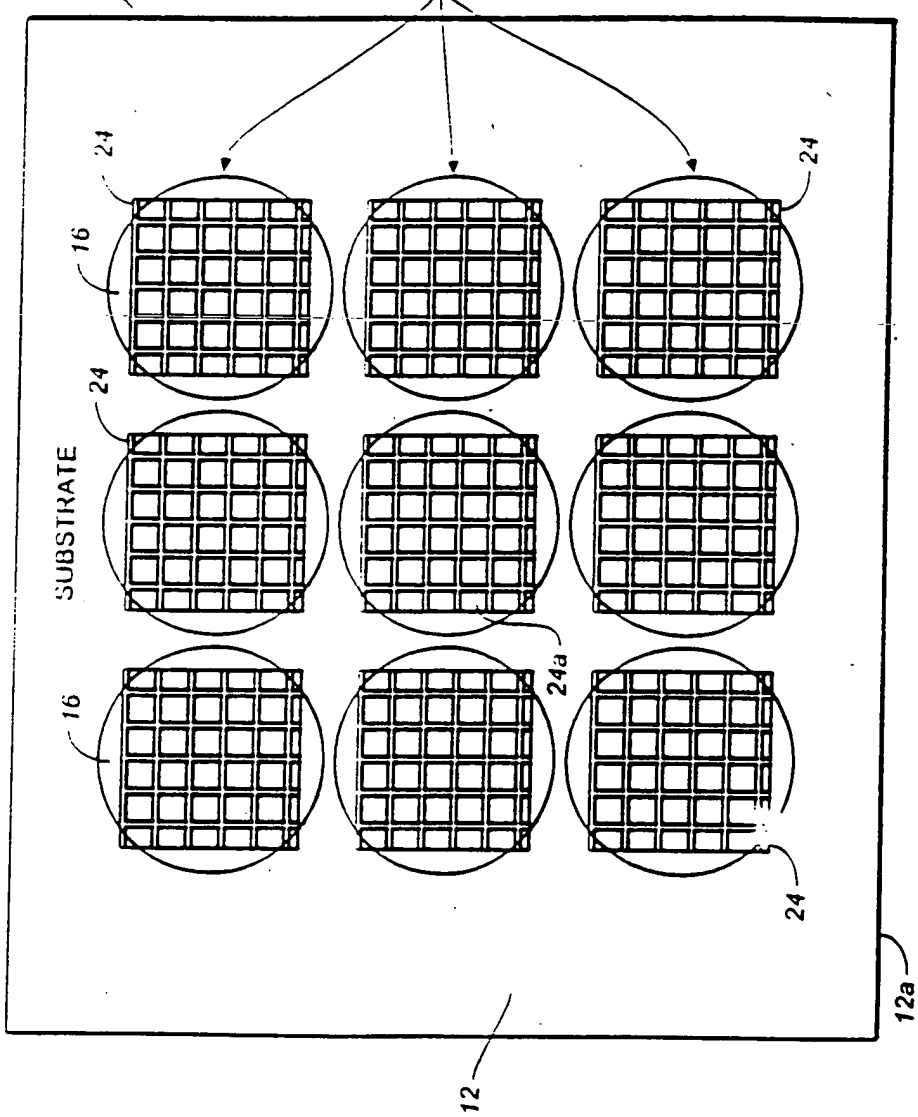


FIG._4

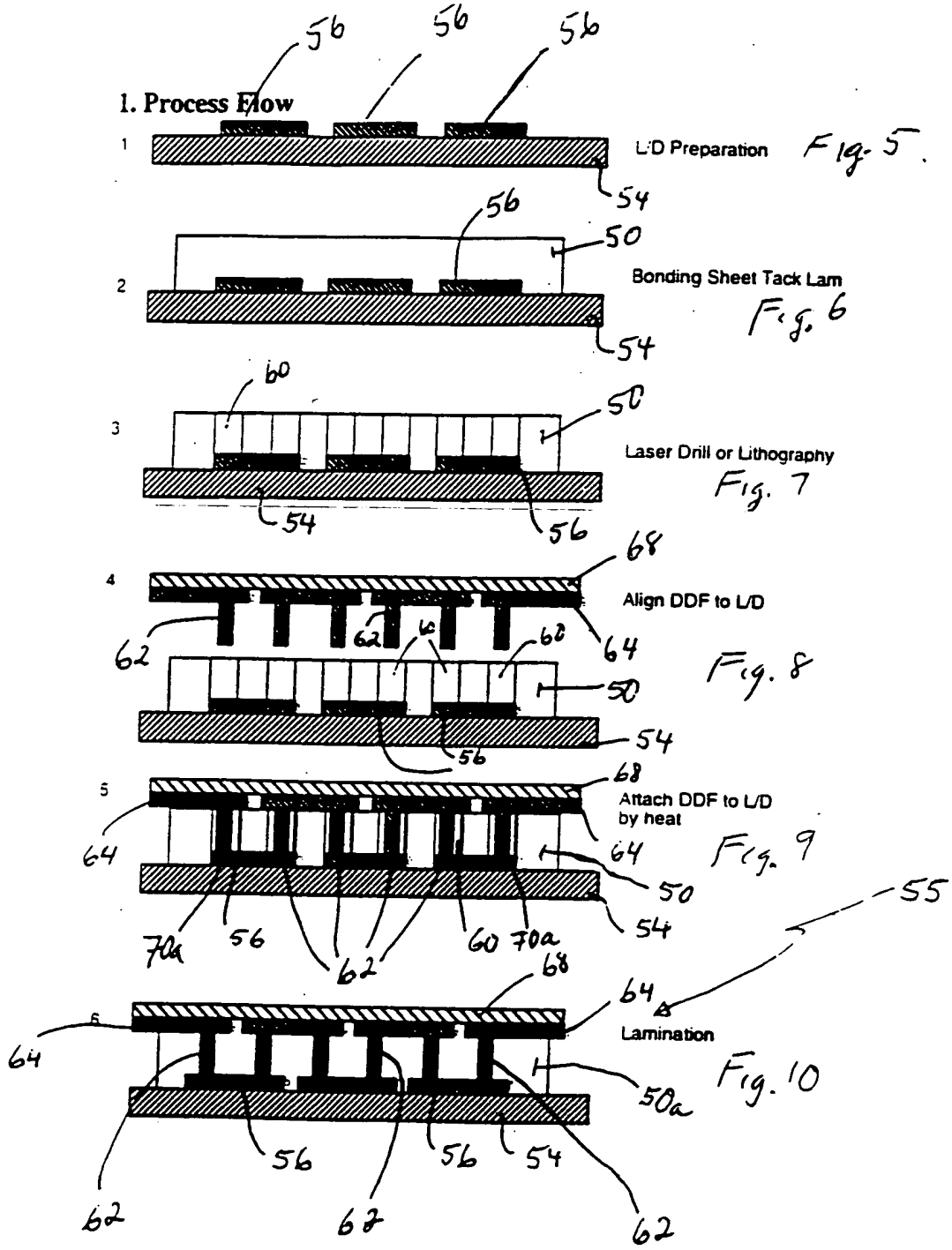


Fig. 5

Fig. 6

Fig. 7

Fig. 8

Fig. 9

Fig. 10

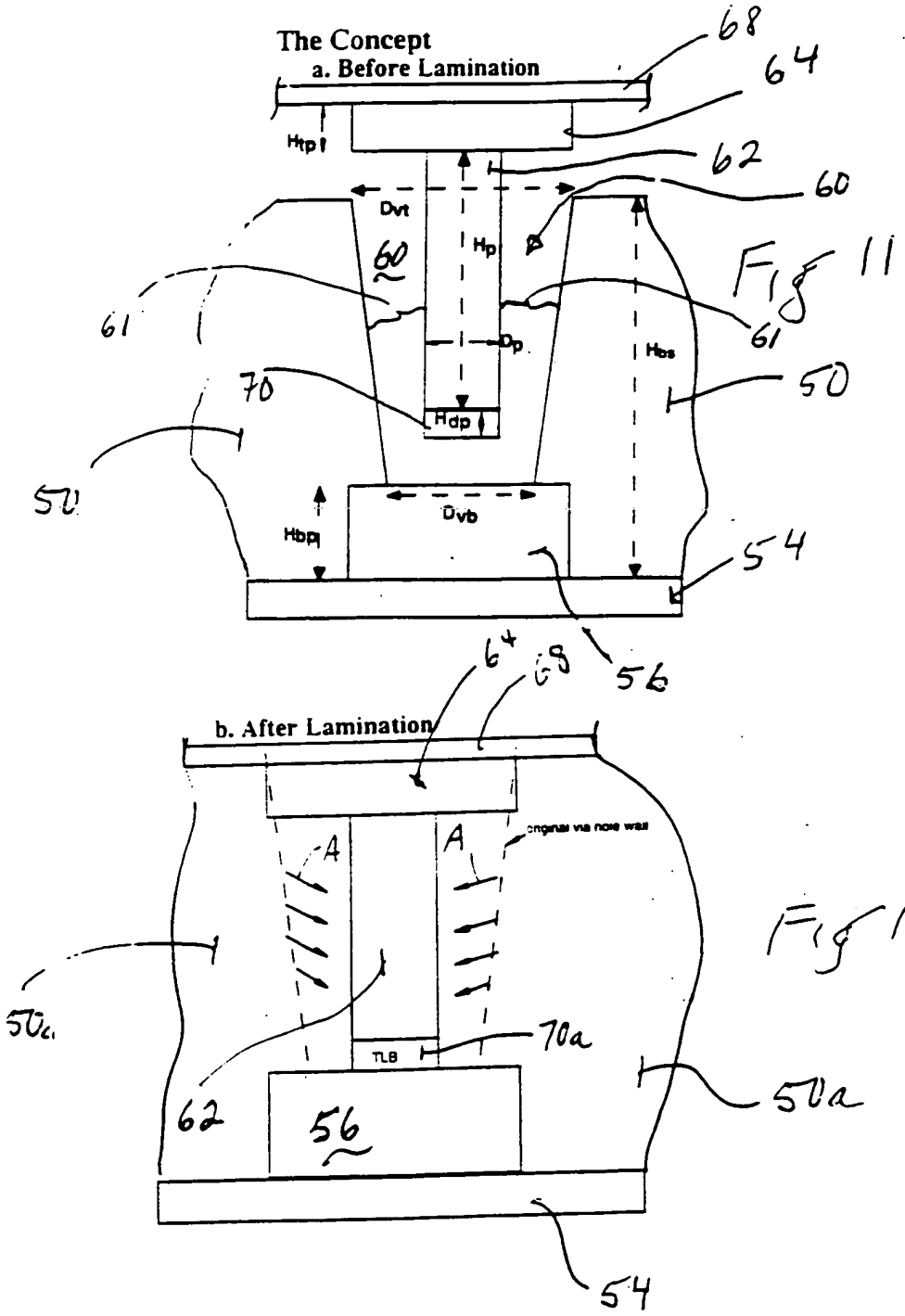

The Concept
a. Before Lamination
68
64
Htp
62
60
Dvt
Hp
60
61
61
Dp
Hbs
70
50
Hdp
50
Dvb
Hbp
54
56
64
68
b. After Lamination
A
A
original via hole wall
50a
70a
TLB
62
56
50a
54

Fig 11

Fig 12

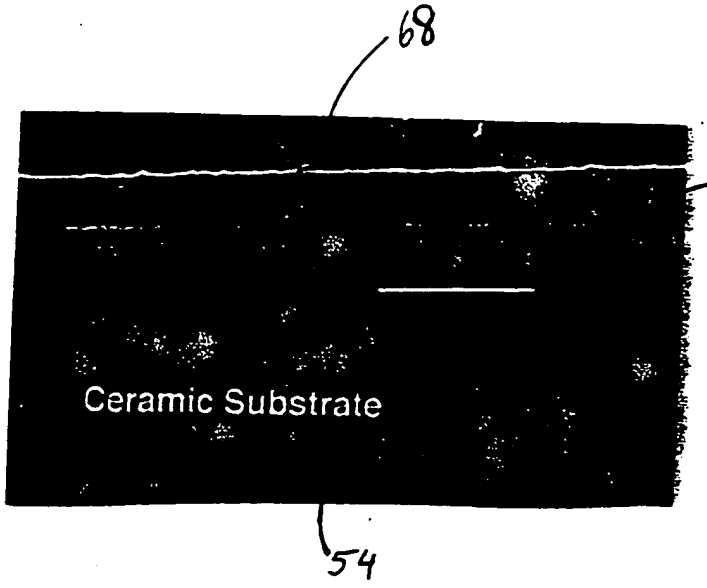

68
50
Ceramic Substrate
54

Fig 13

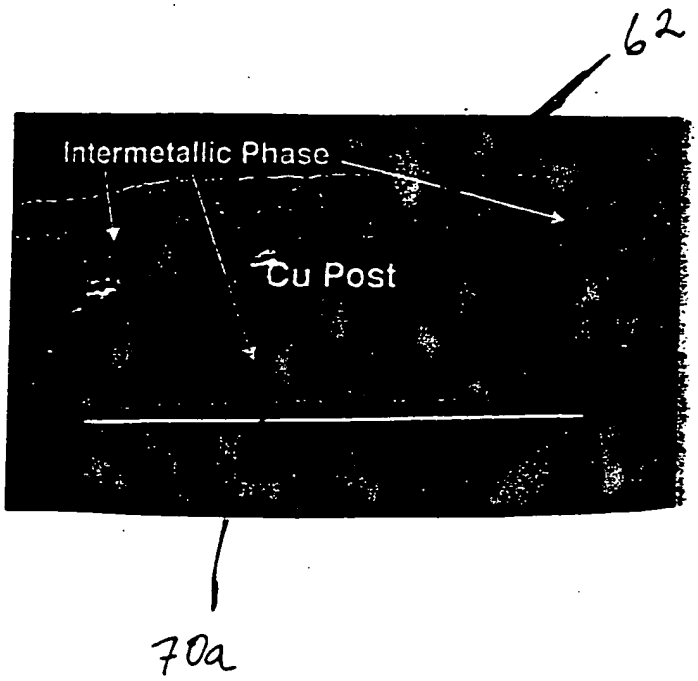

62
Intermetallic Phase
Cu Post
70a

Fig 14

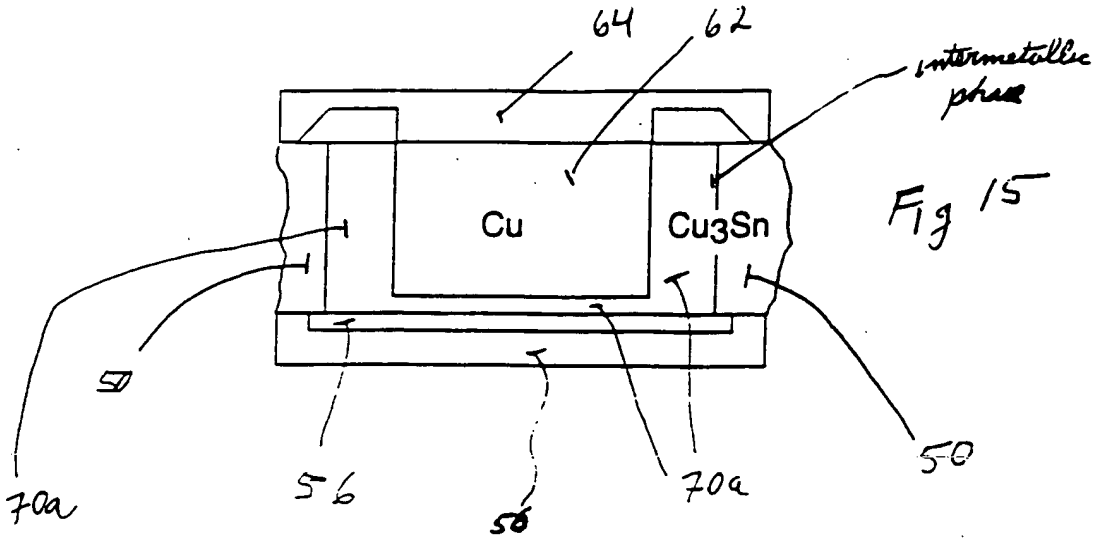

64
62
intermetallic phase
Cu
Cu3Sn
70a
56
58
70a
50

Fig 15

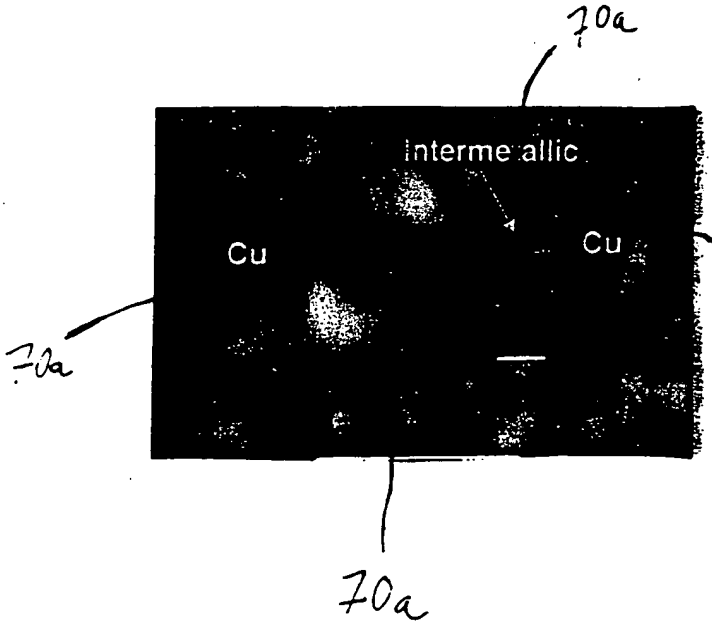

70a
Interme allic
Cu
Cu
70a
70a

Fig 16

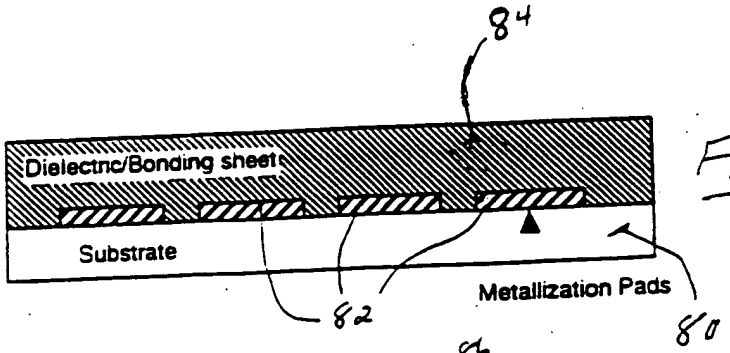


Fig 17

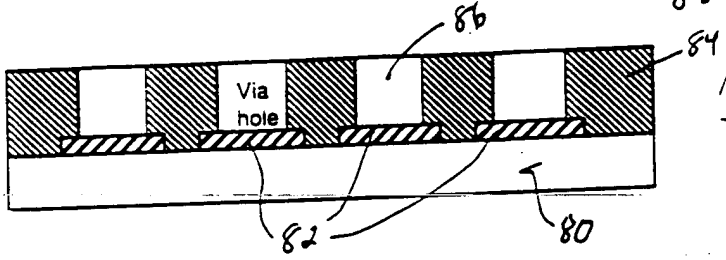


Fig 18

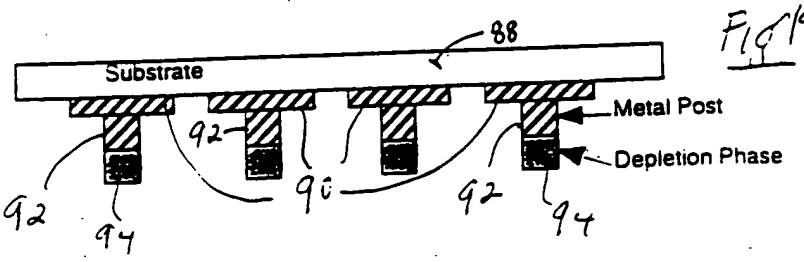


Fig 19

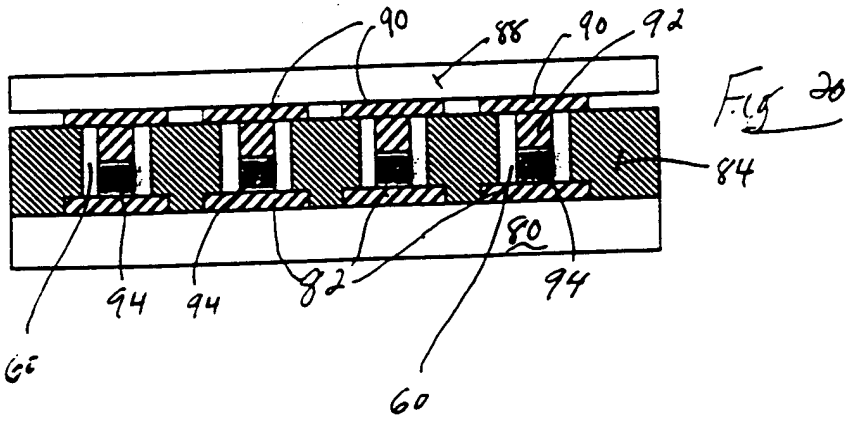


Fig 20

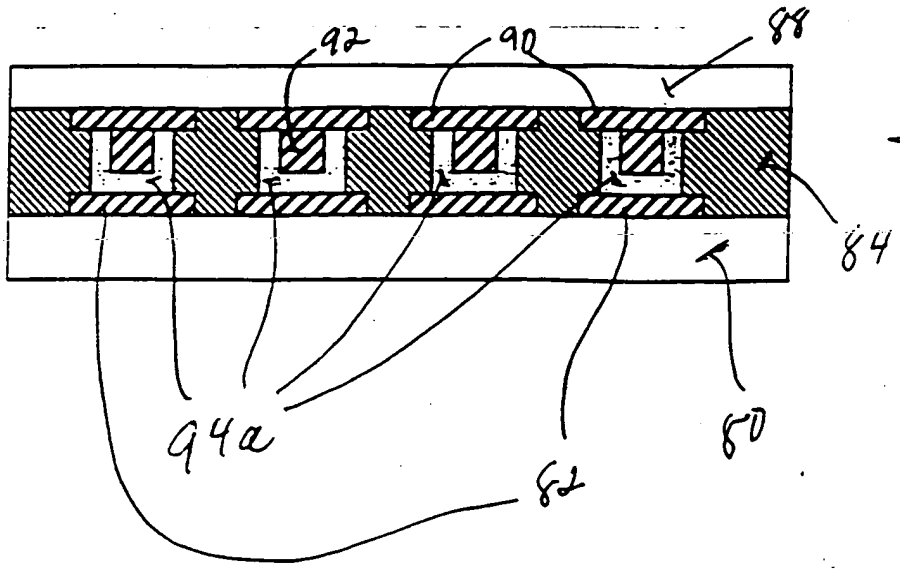


Fig 21

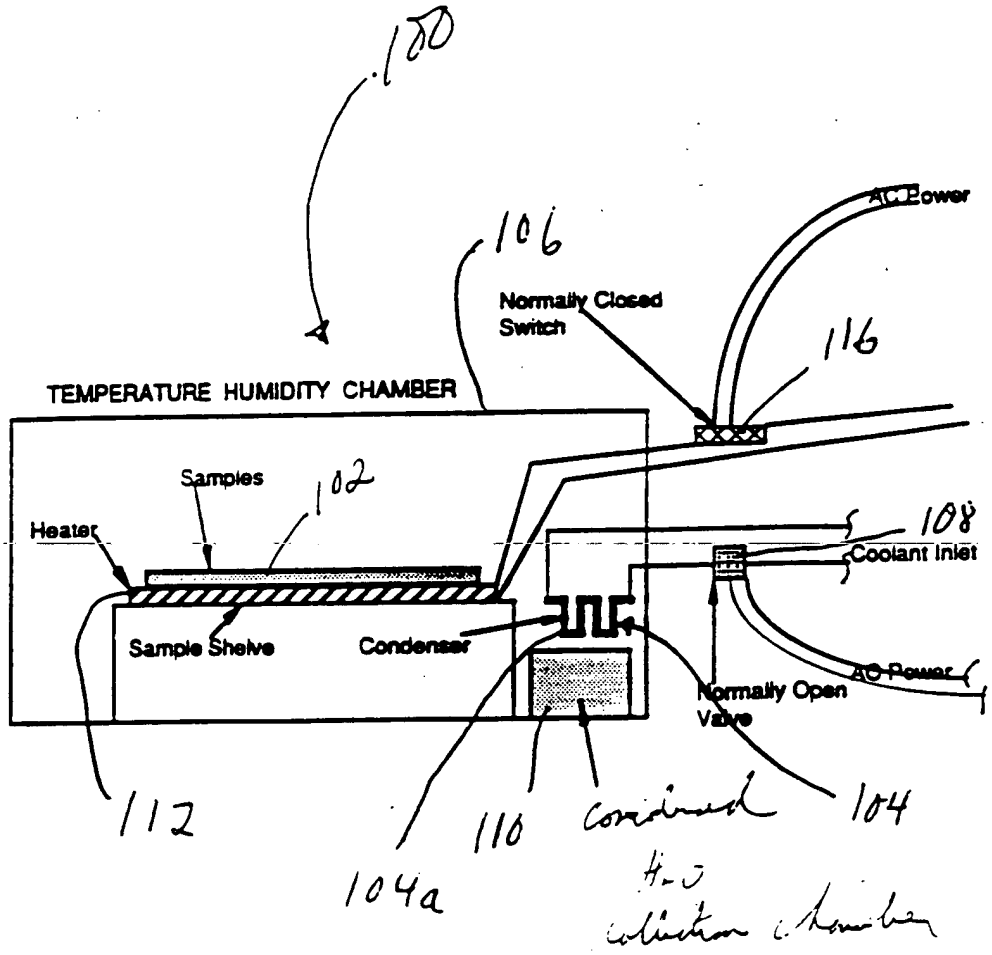

100
106
AC Power
Normally Closed Switch
116
TEMPERATURE HUMIDITY CHAMBER
Samples
102
Heater
108
Coolant Inlet
Sample Shelve
Condenser
AC Power
Normally Open Valve
112
110
104
104a
condenser
H-3
vibration chamber

Fig 22

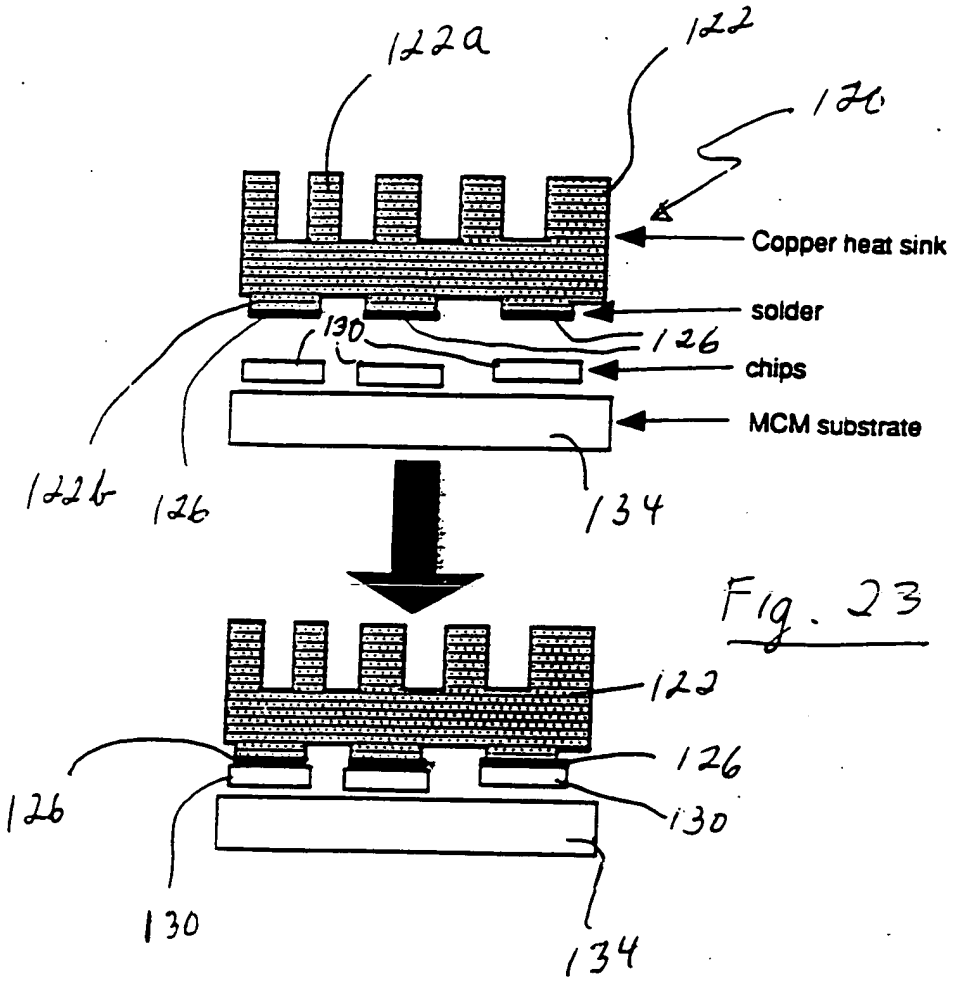

122a
122
120
Copper heat sink
solder
130
126
chips
MCM substrate
122b
126
134
122
126
126
130
130
134

Fig. 23

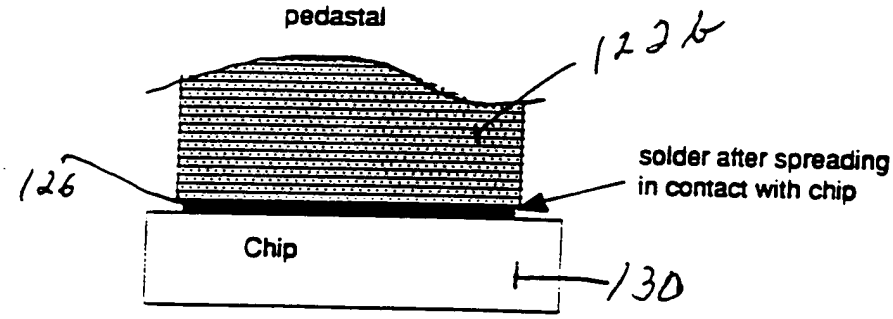

pedastal
122b
126
solder after spreading
in contact with chip
Chip
130

Fig 24

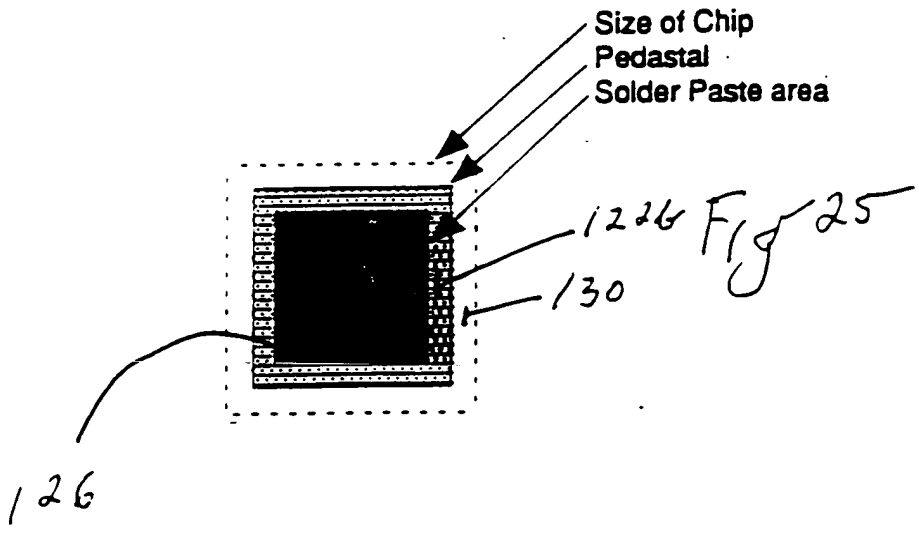
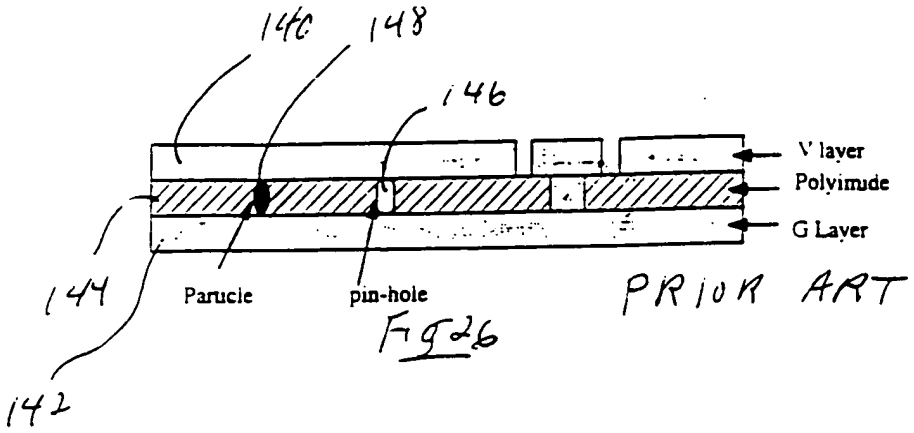


Fig 25



PRIOR ART

Fig 26

The New Process

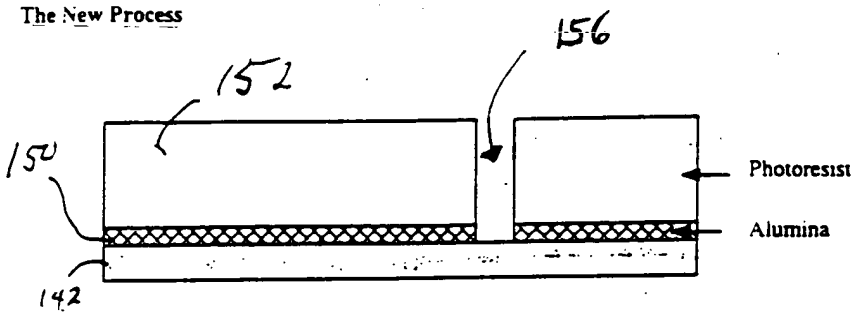


Fig 27

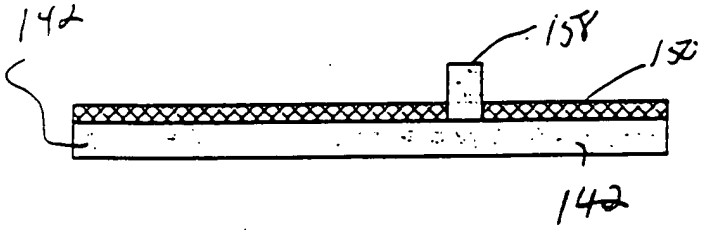


Fig 28

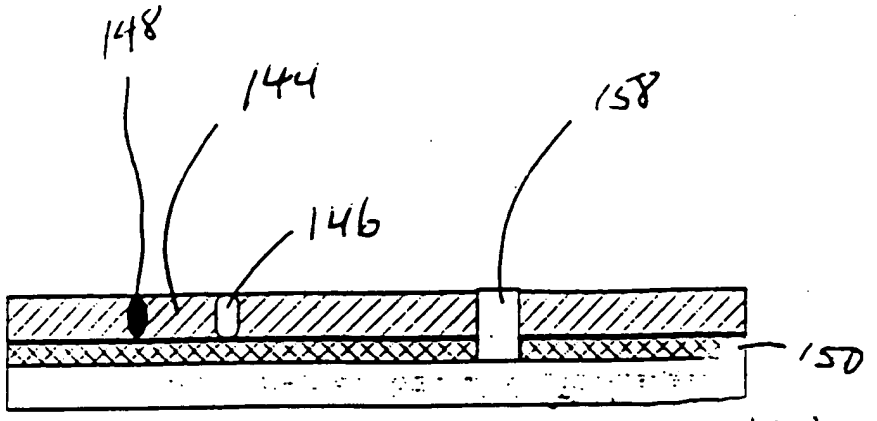


Fig 29

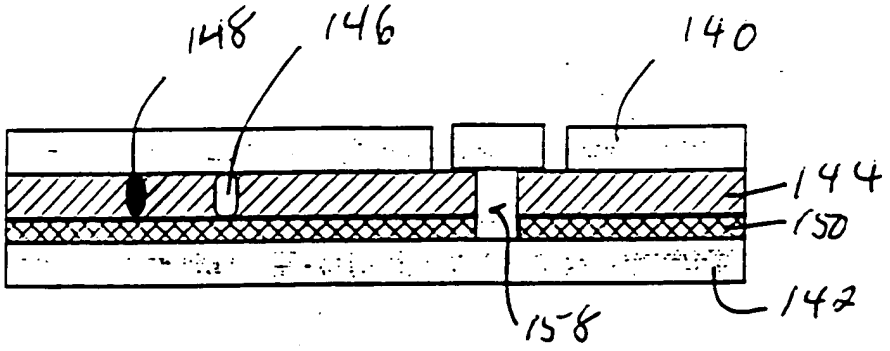


Fig 30

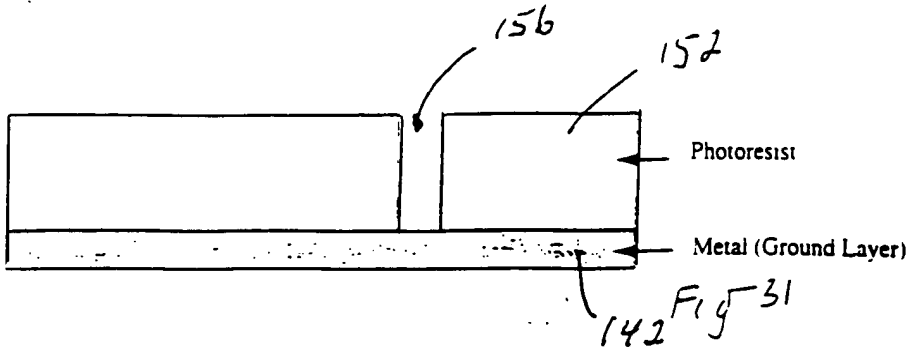


Fig 31

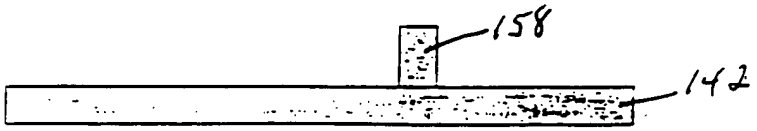


Fig 32

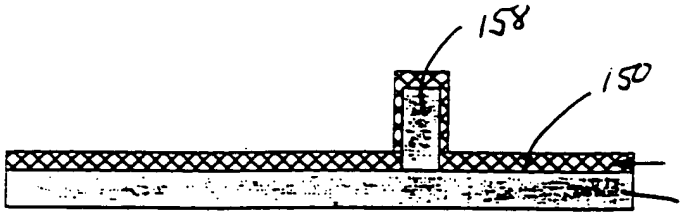


Fig 33

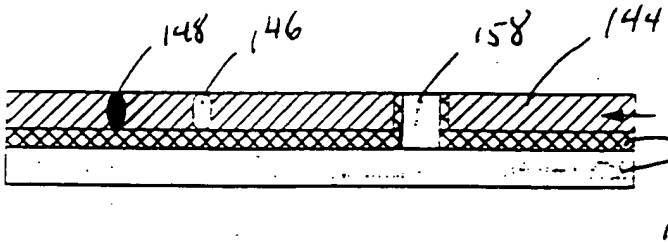


Fig 34

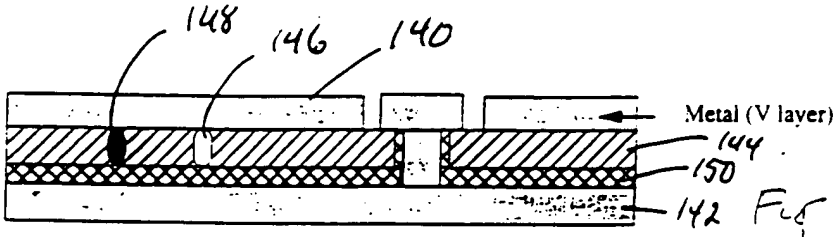


Fig 35

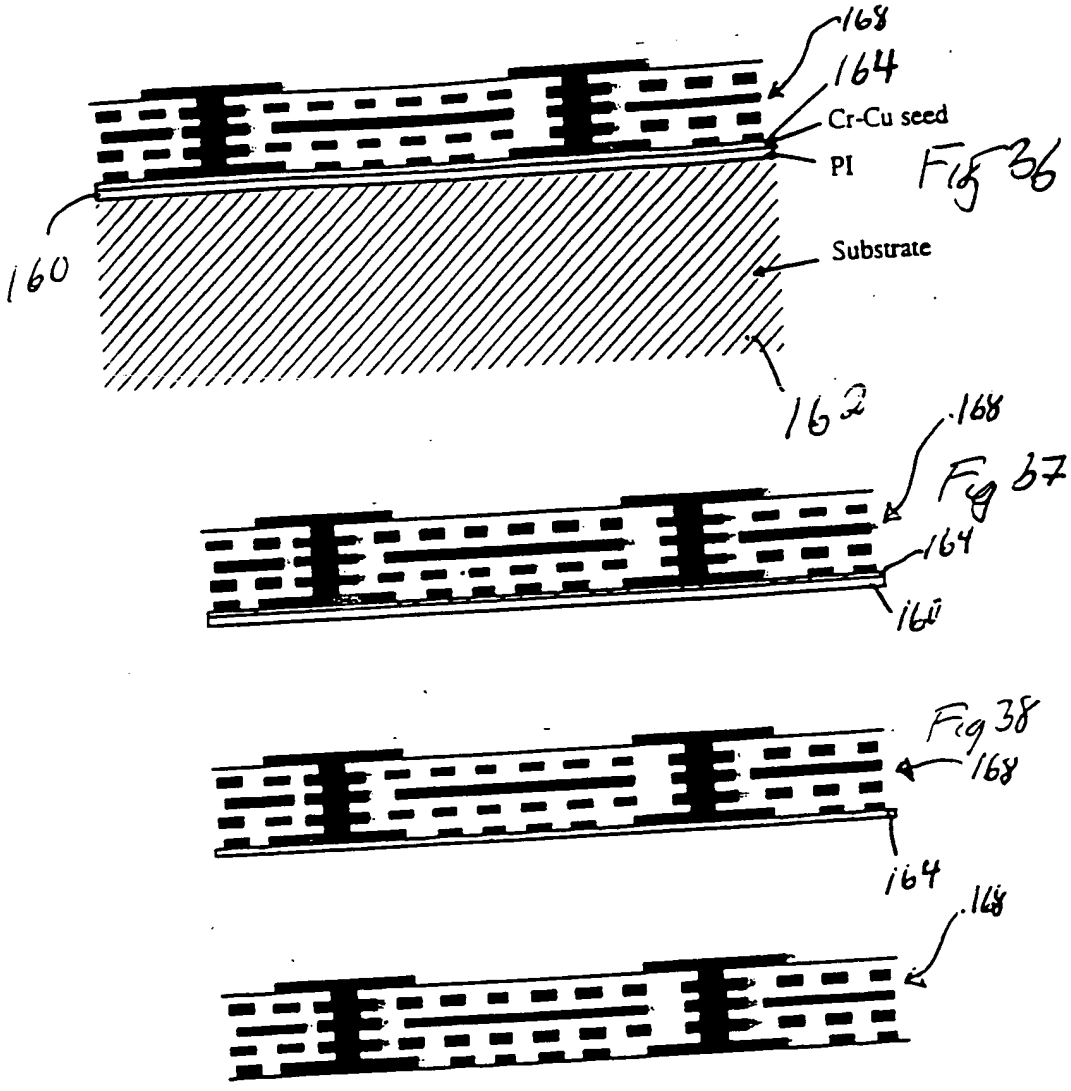


Fig 36

Fig 37

Fig 38

Fig 39

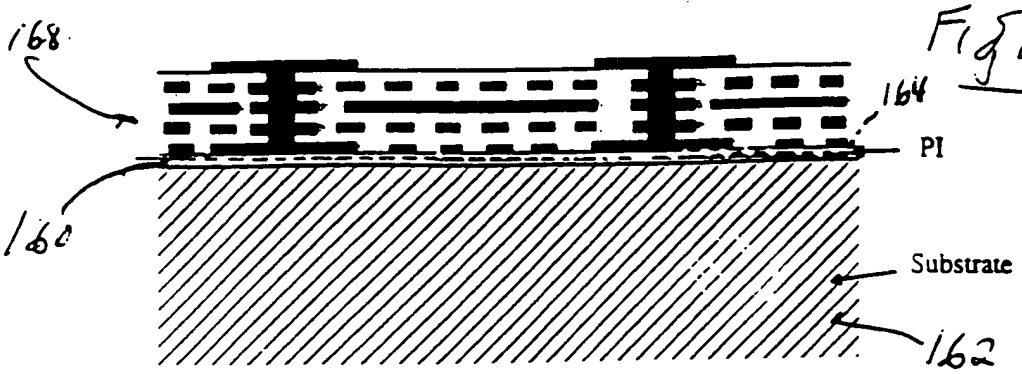


Fig 40

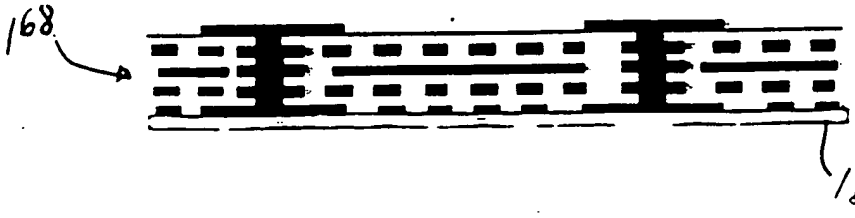


Fig 41

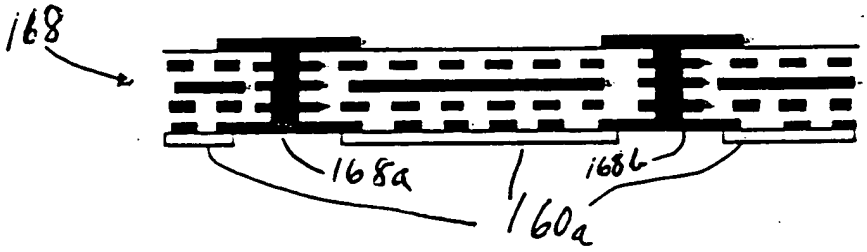


Fig 42

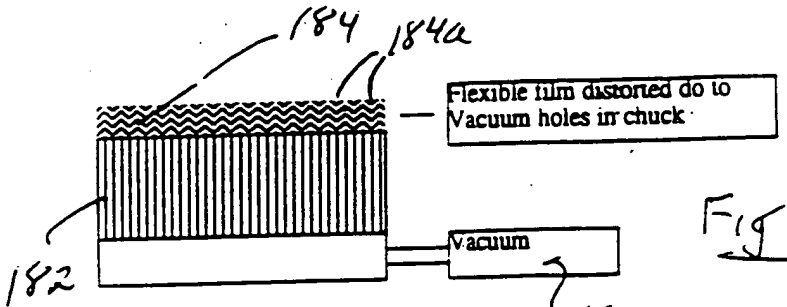


Fig 43

Figure 1

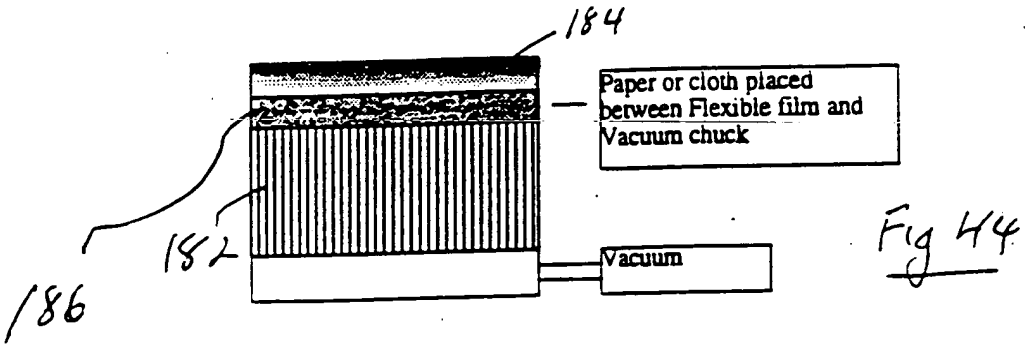


Fig 44

Figure 2

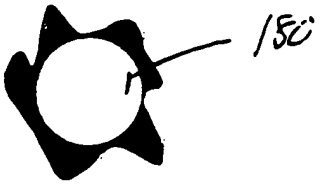


Figure 3

Fig 45

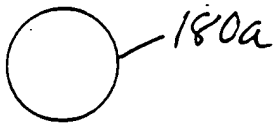


Figure 4

Fig 46

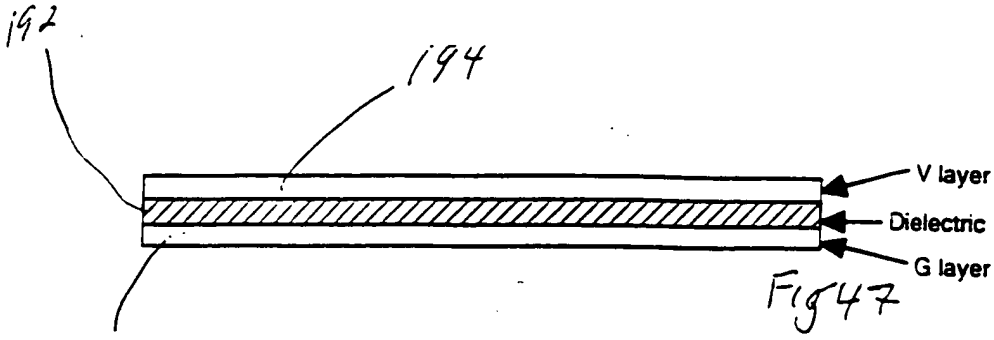


Fig 47

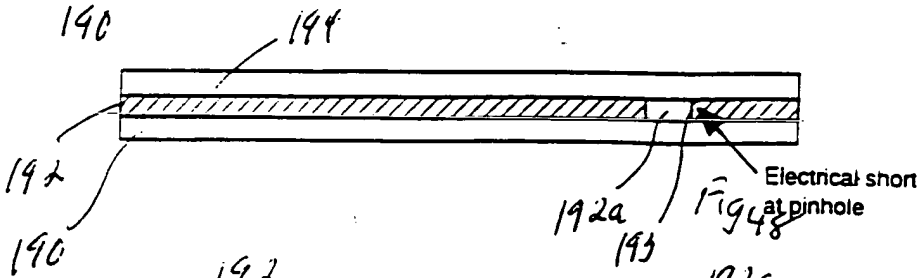


Fig 48

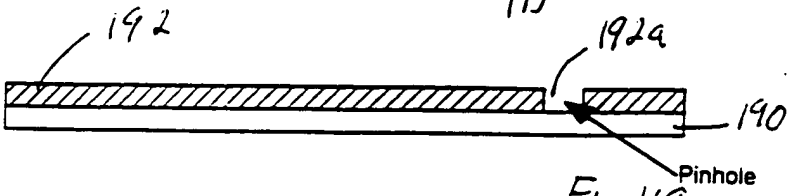


Fig 49

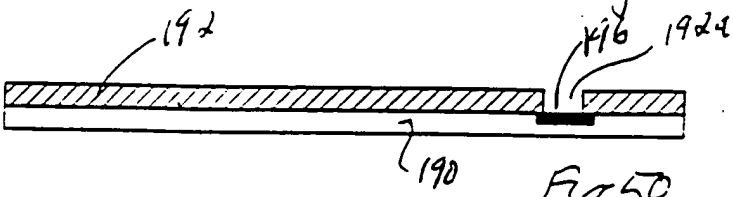


Fig 50

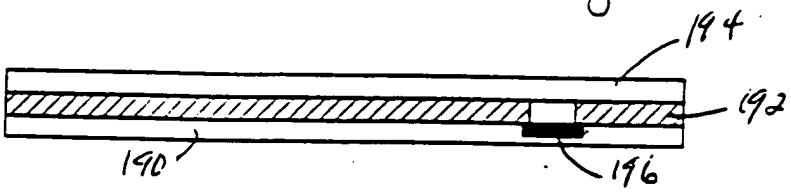


Fig 51

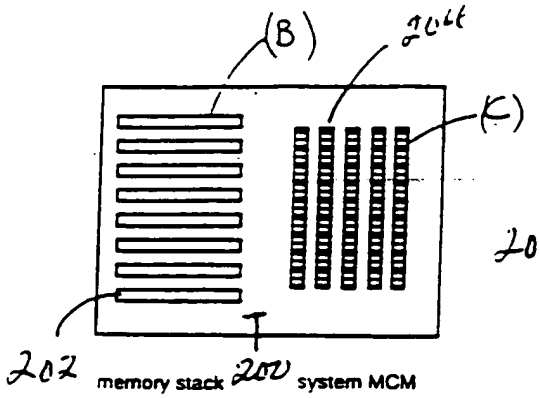


Fig 52A

Case (I)

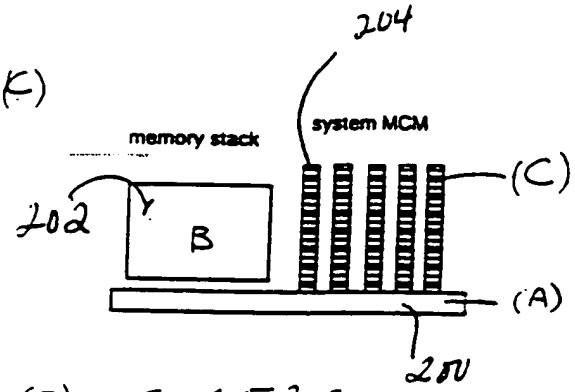


Fig 52B

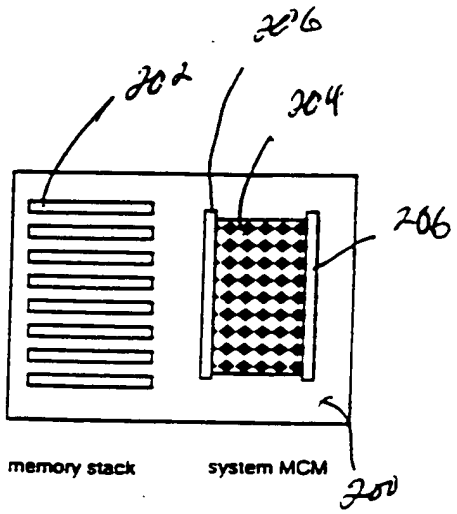


Fig 53A

Case (II)

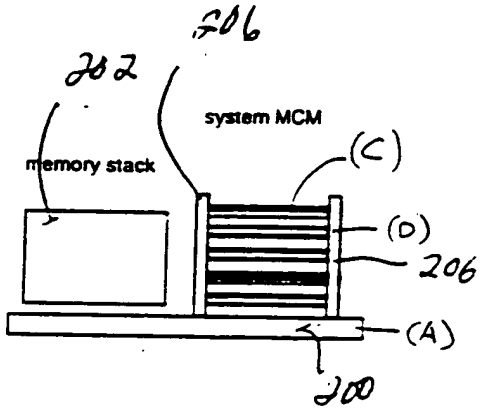


Fig 53B

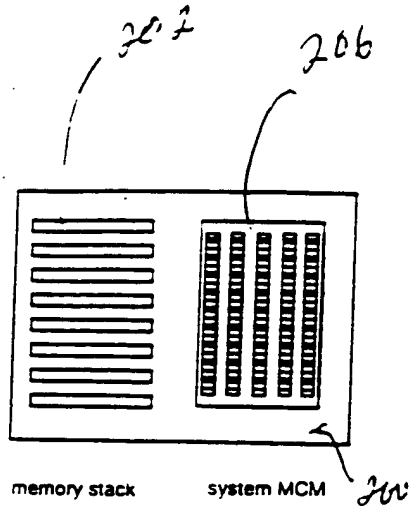


Fig 54A

Case (III)

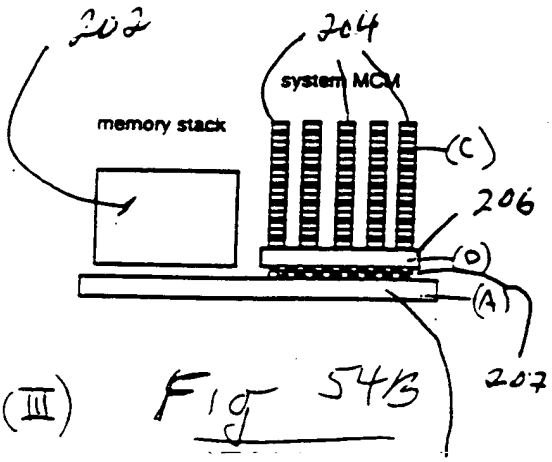


Fig 54B

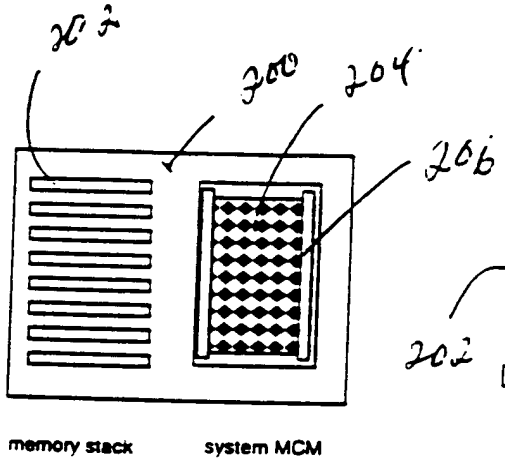


Fig 55A

Case (IV)

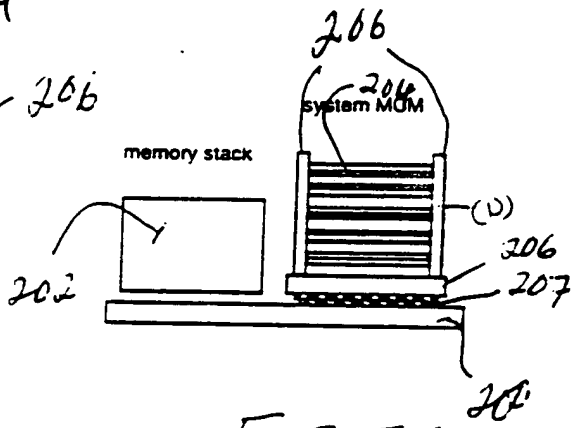


Fig 55B

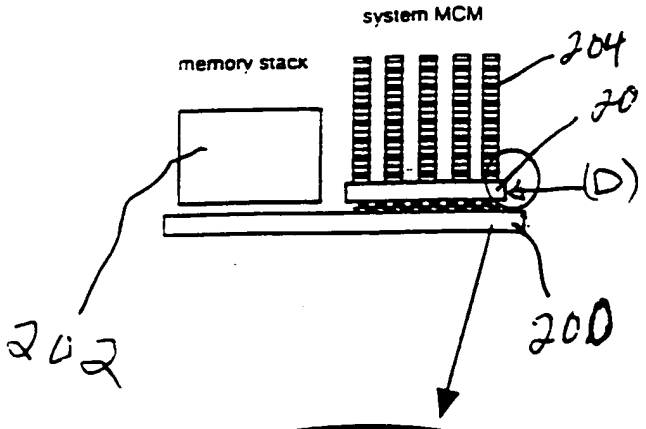

system MCM
memory stack
204
206
(D)
202
200

Fig 56

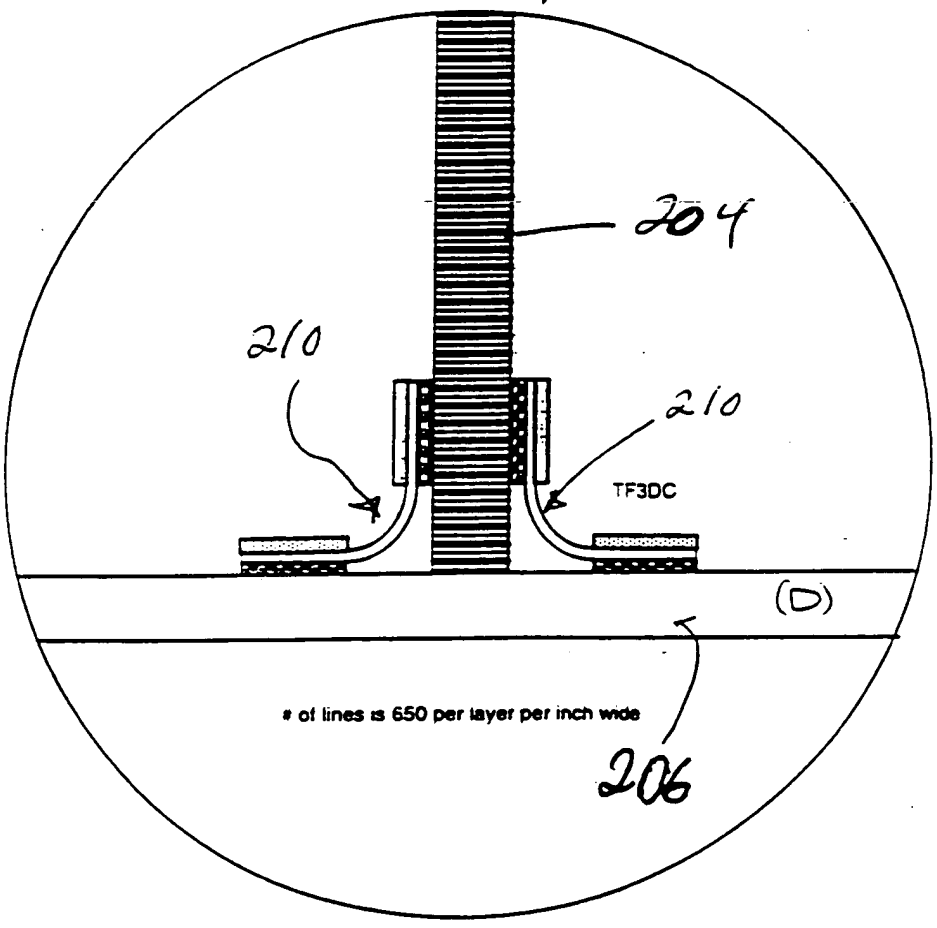

204
210
210
TF3DC
(D)
# of lines is 650 per layer per inch wide
206

Fig 57

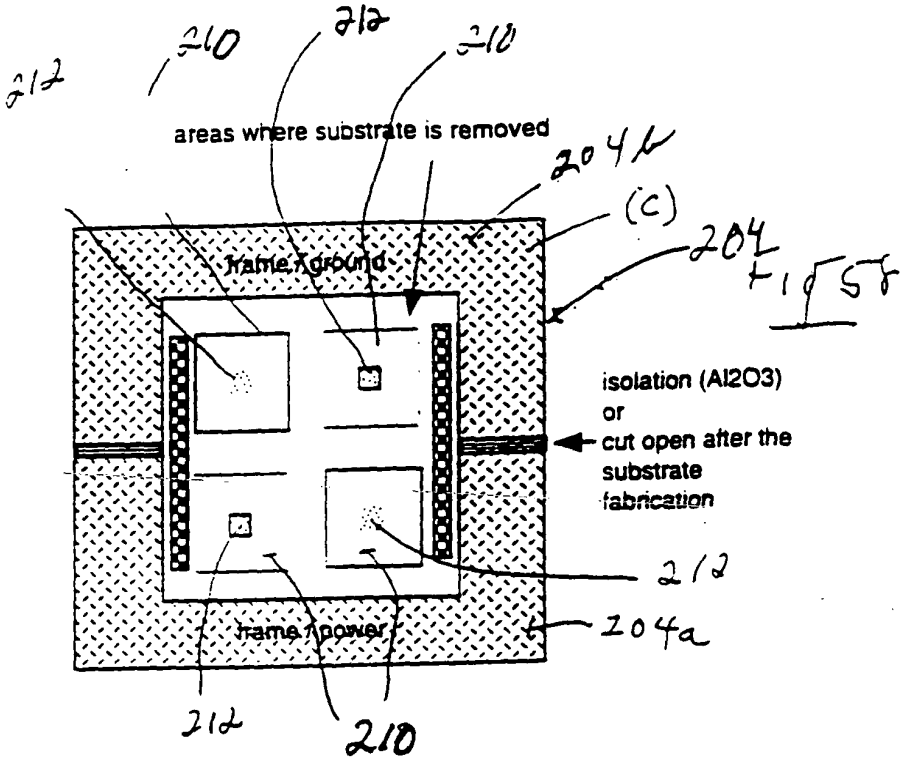


Fig 58

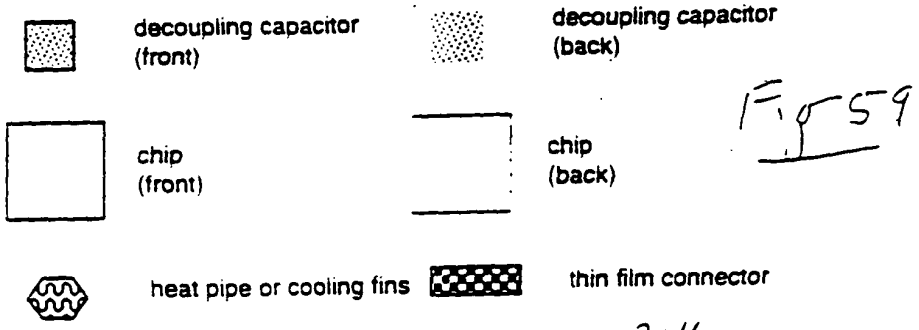


Fig 59

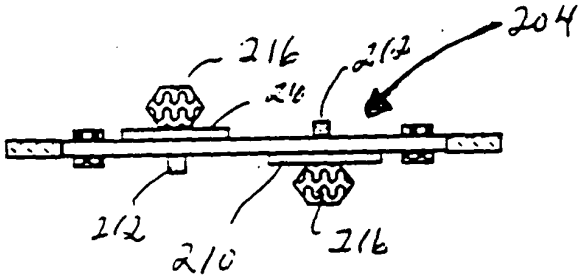


Fig 60

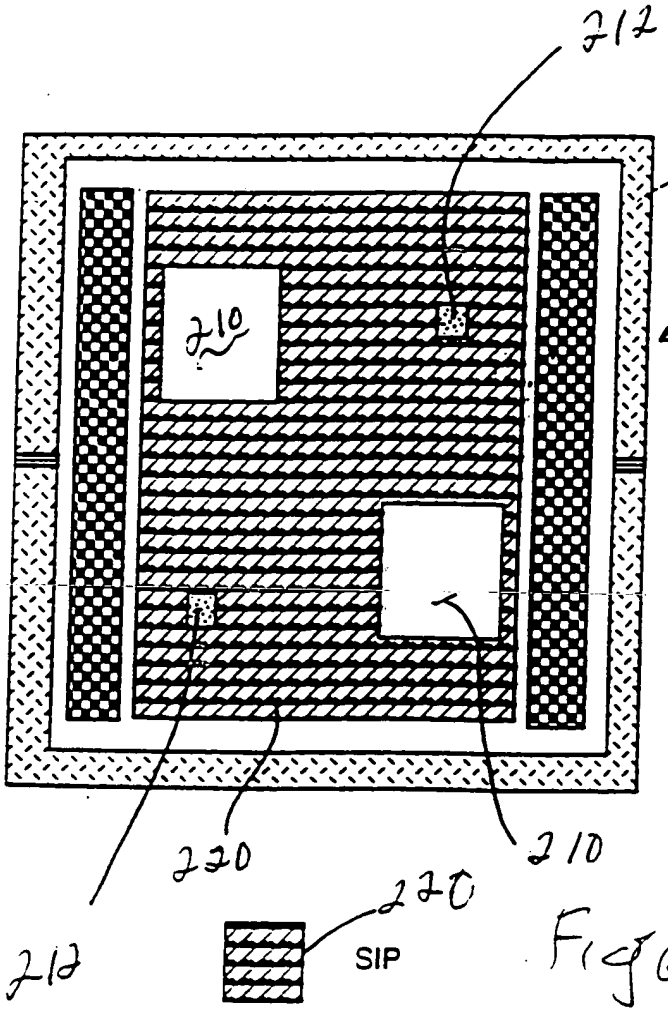


Fig 6a

Fig 6b

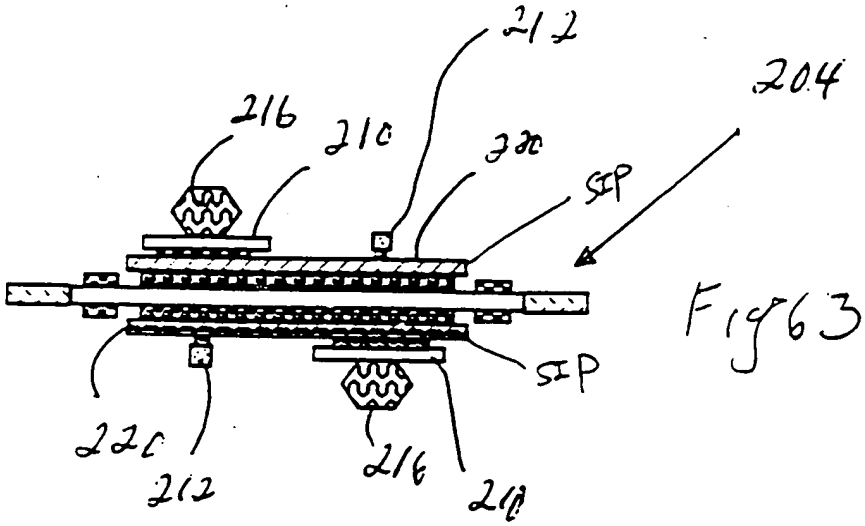
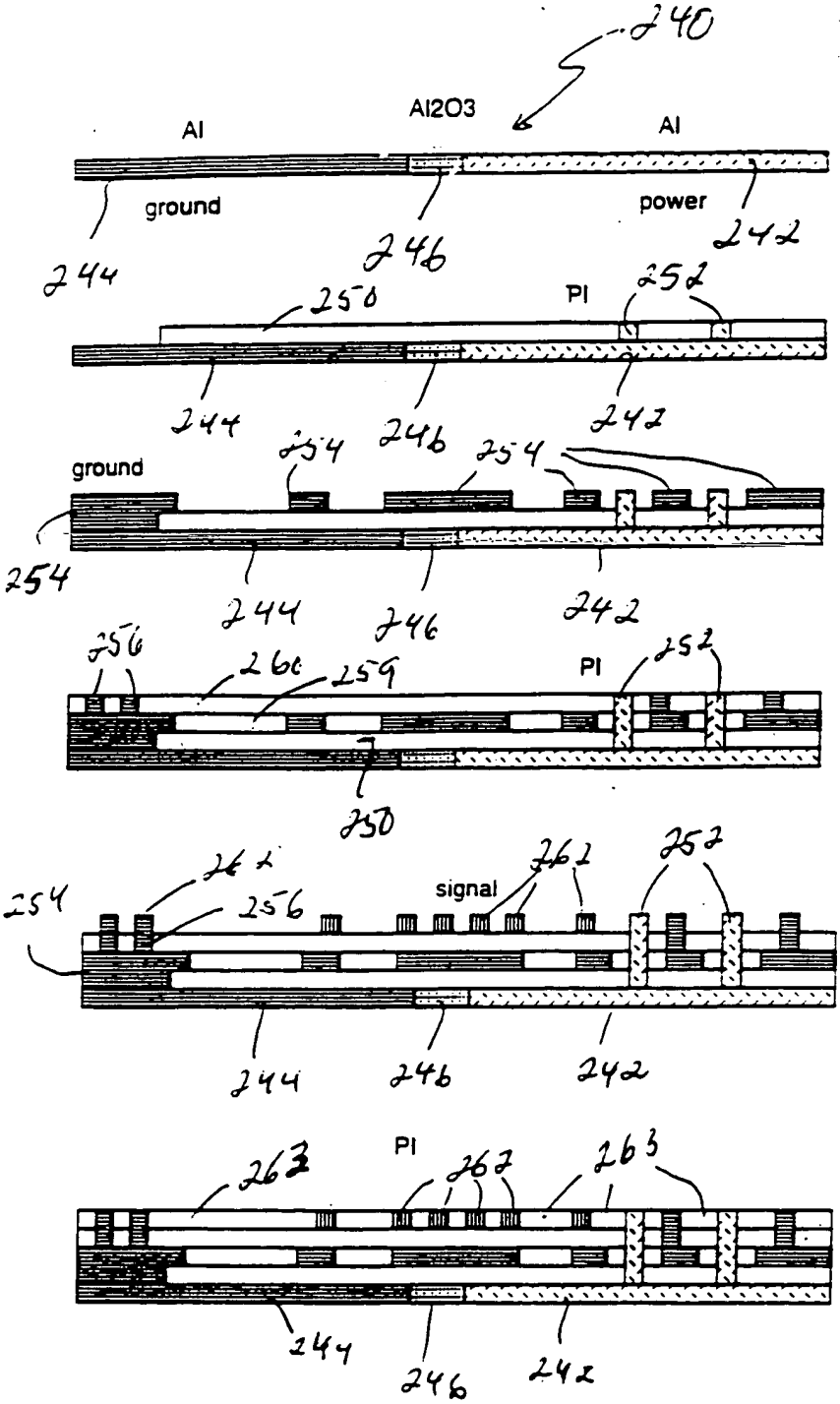


Fig 6c


240
Al2O3
Al
Al
ground
power
244
246
242
Fig 64
250
PI
252
Fig 65
254
ground
Fig 66
256
260
259
Fig 67
262
signal
261
Fig 68
263
267
Fig 69

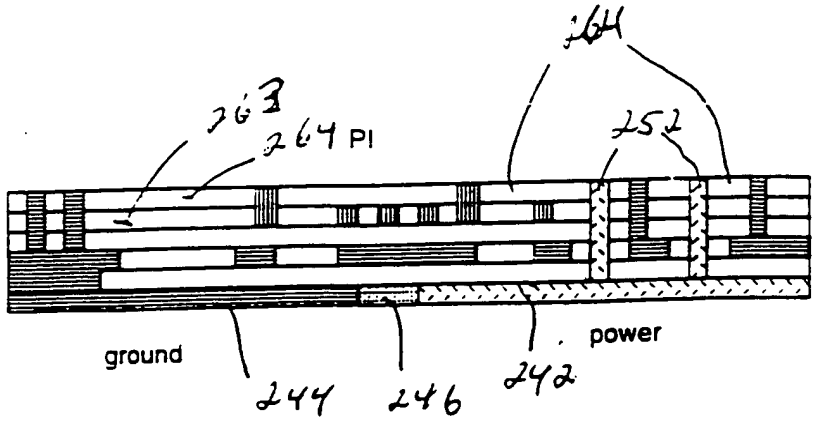


Fig 70

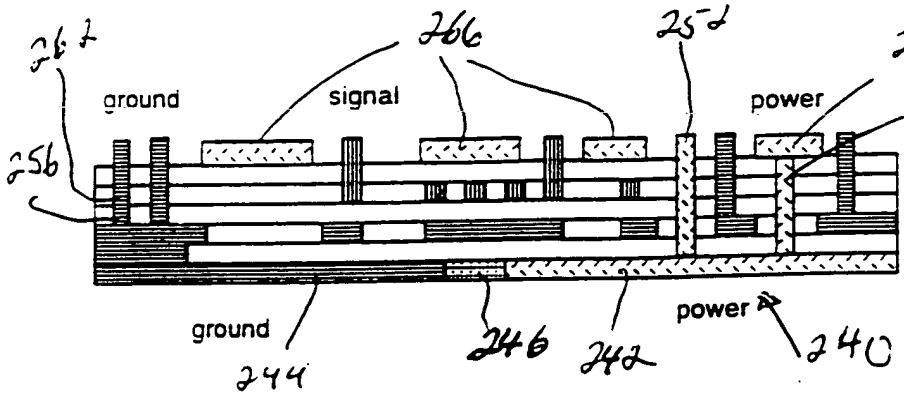


Fig 71

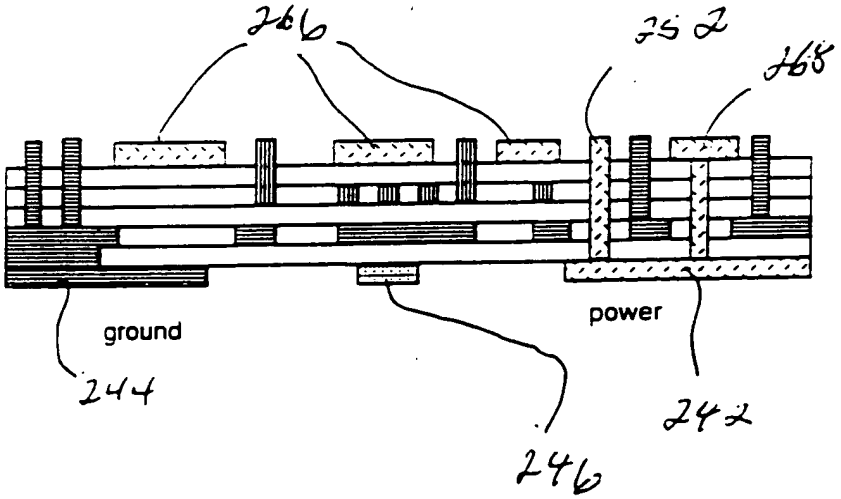


Fig 72

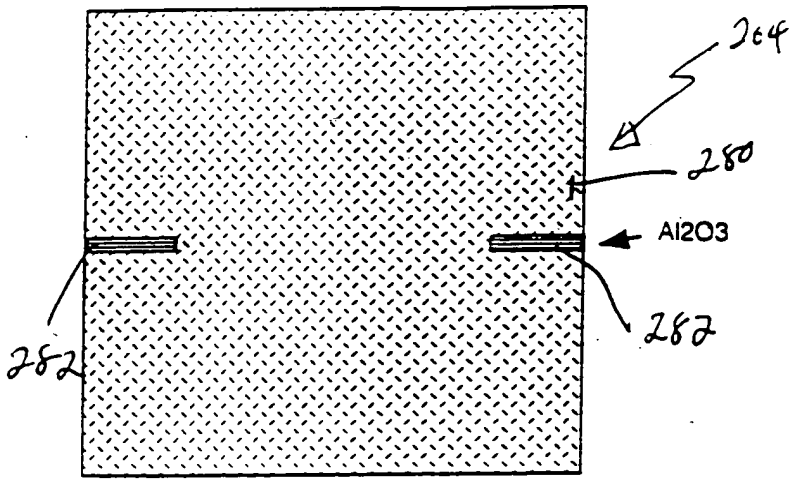


Fig. 73

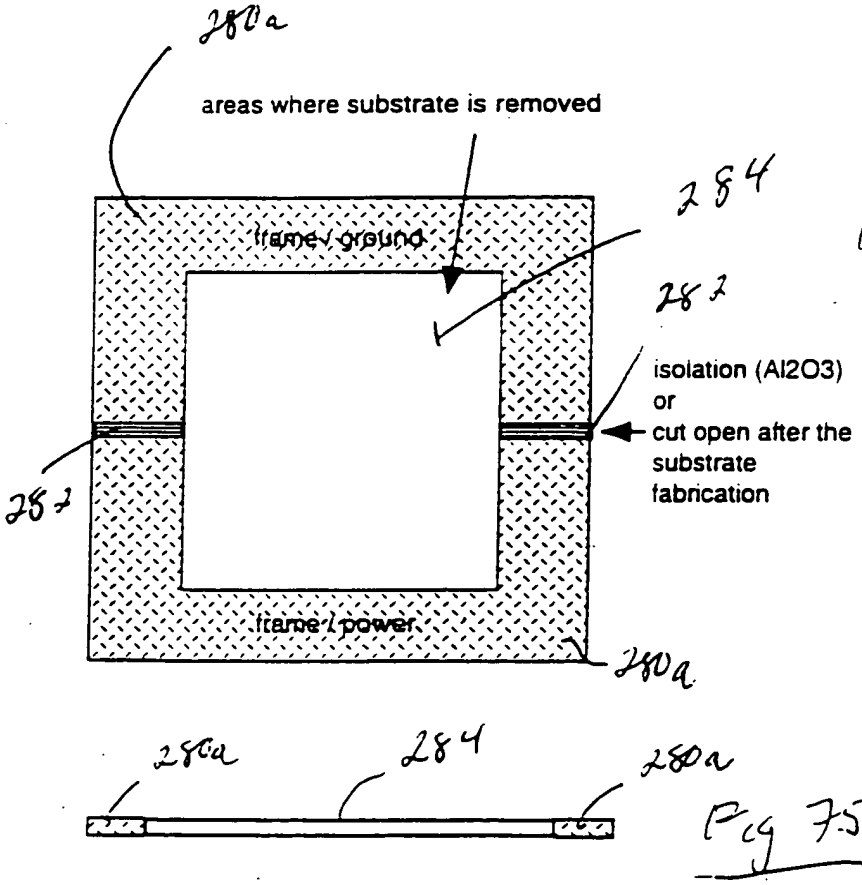


Fig. 74

Fig 75

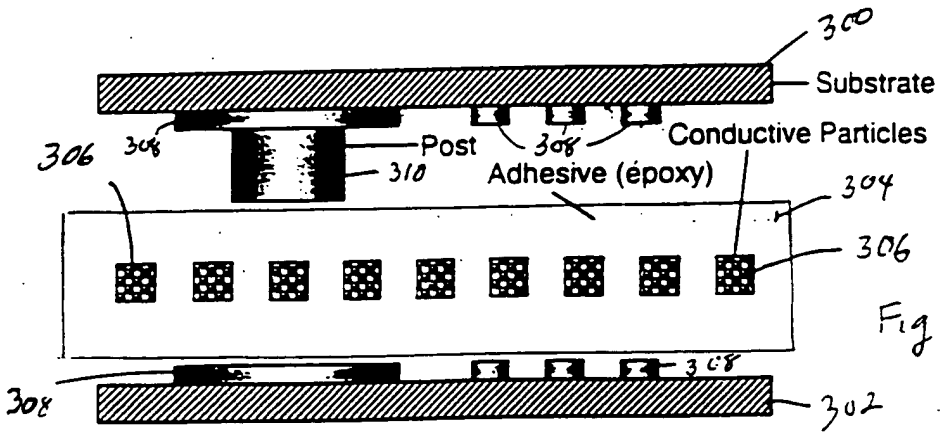

300
Substrate
306
308
Post
310
308
Conductive Particles
Adhesive (epoxy)
304
306
308
308
302

Fig. 76

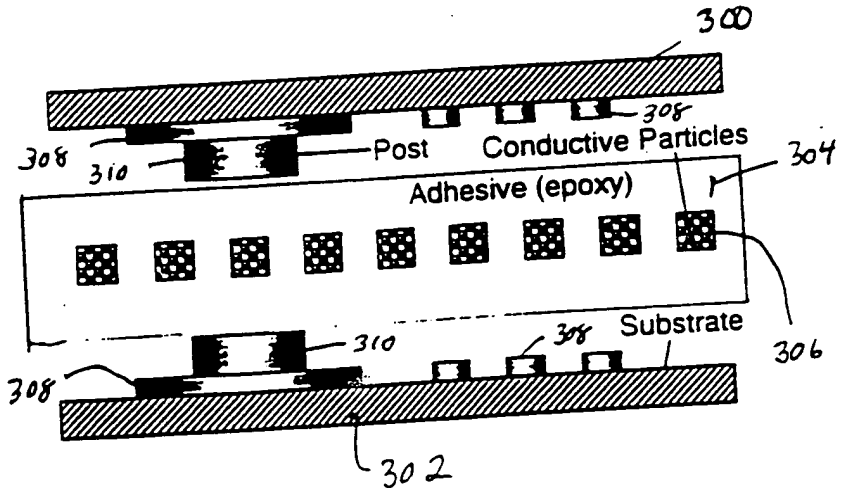

300
308
308
310
Post
Conductive Particles
304
Adhesive (epoxy)
306
310
308
Substrate
308
302

Fig 77

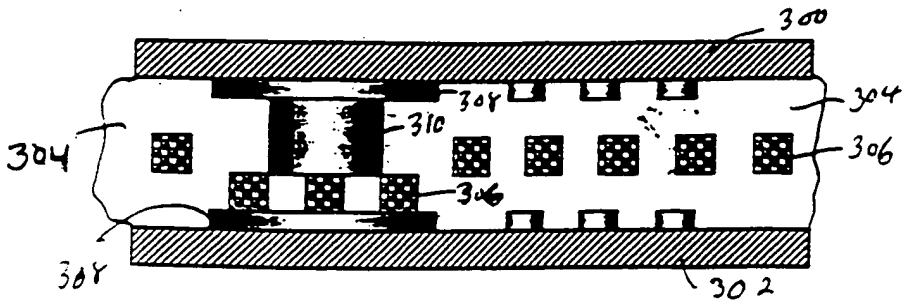


Fig 78

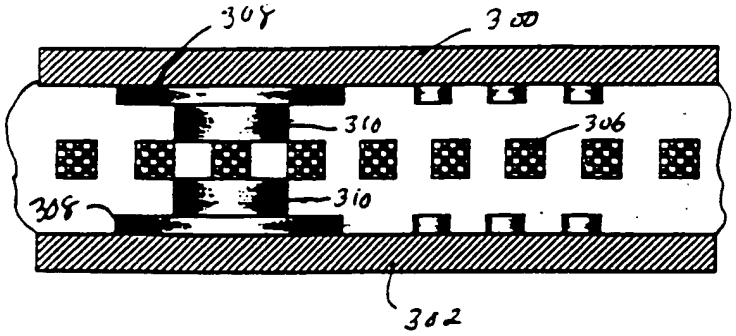


Fig 79

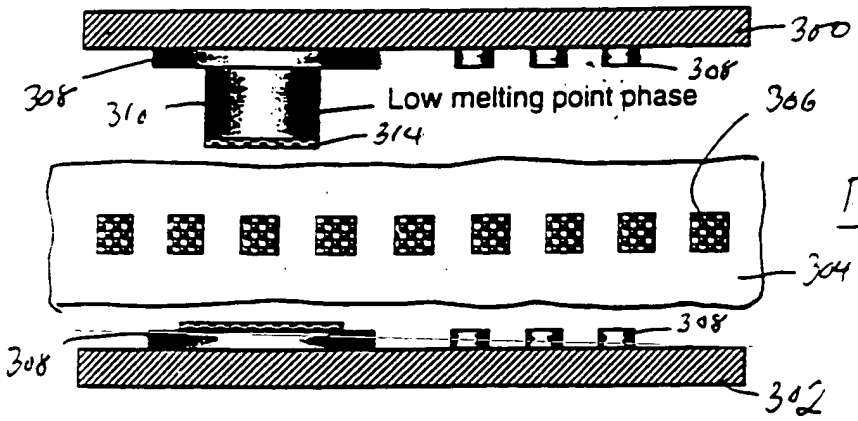

300
308
308
310
Low melting point phase
314
306
304
308
308
302

Fig 8C

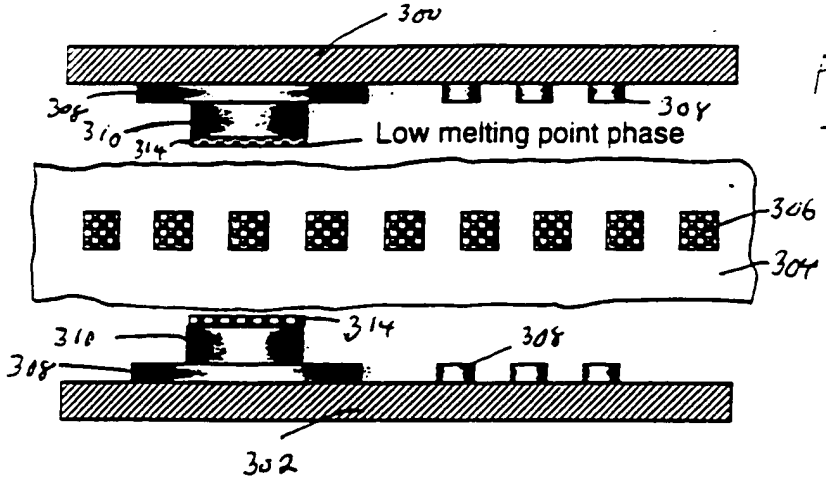

300
308
310
314
Low melting point phase
306
304
310
314
308
308
302

Fig 8I

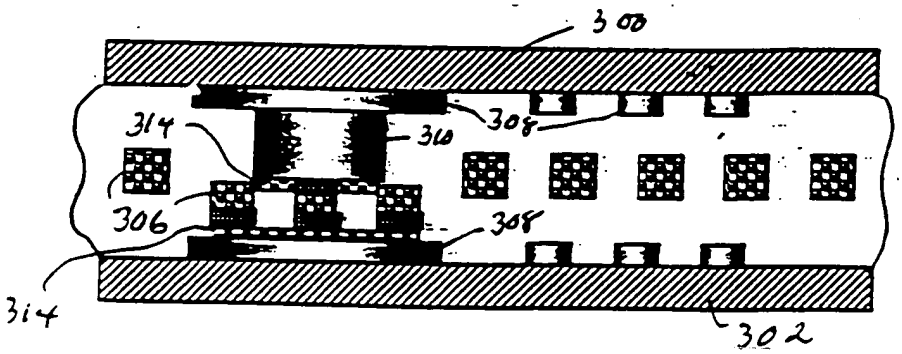

300
314
310
308
306
308
314
302

Fig 82

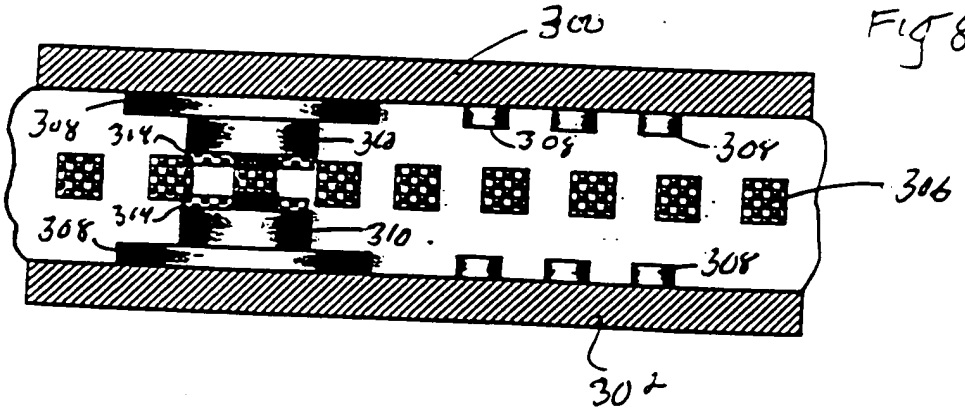

300
308
314
310
308
304
306
308
314
310
308
302

Fig 83

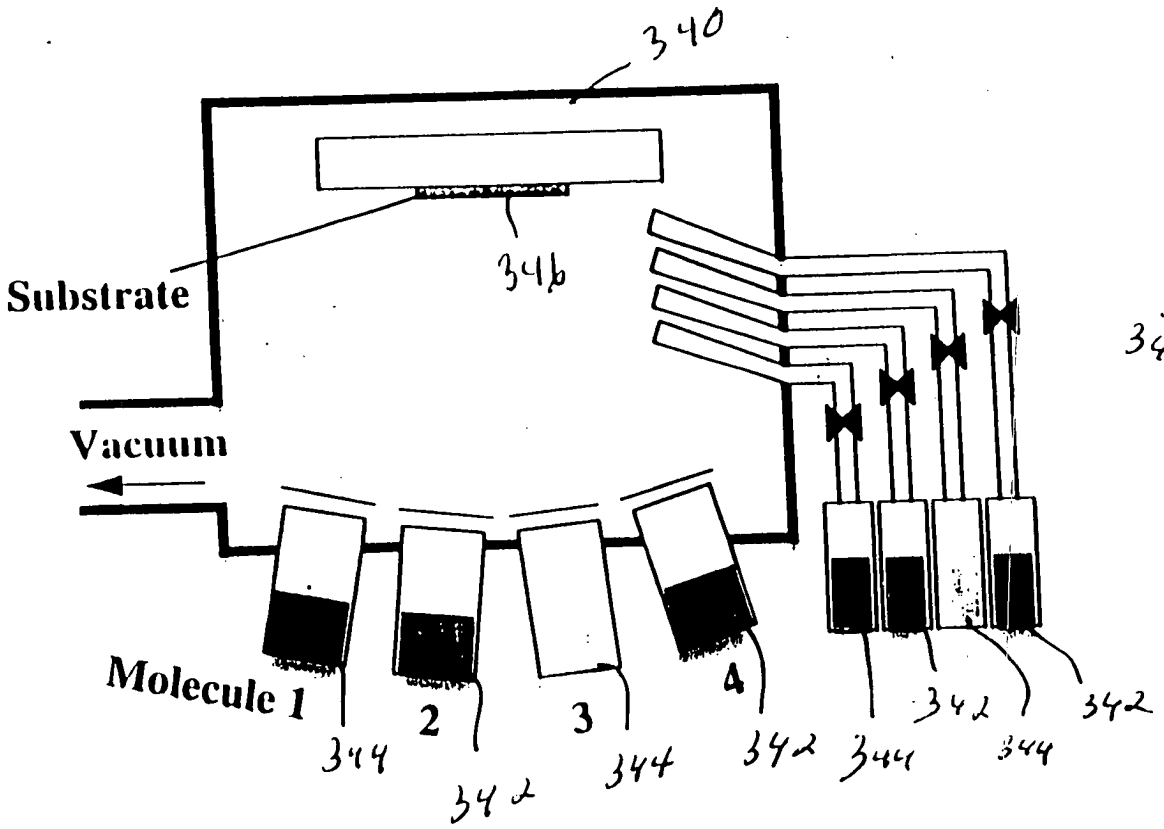


Fig 84A

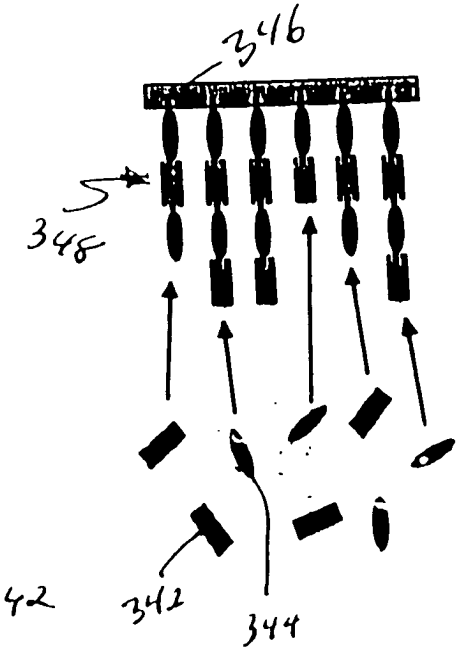
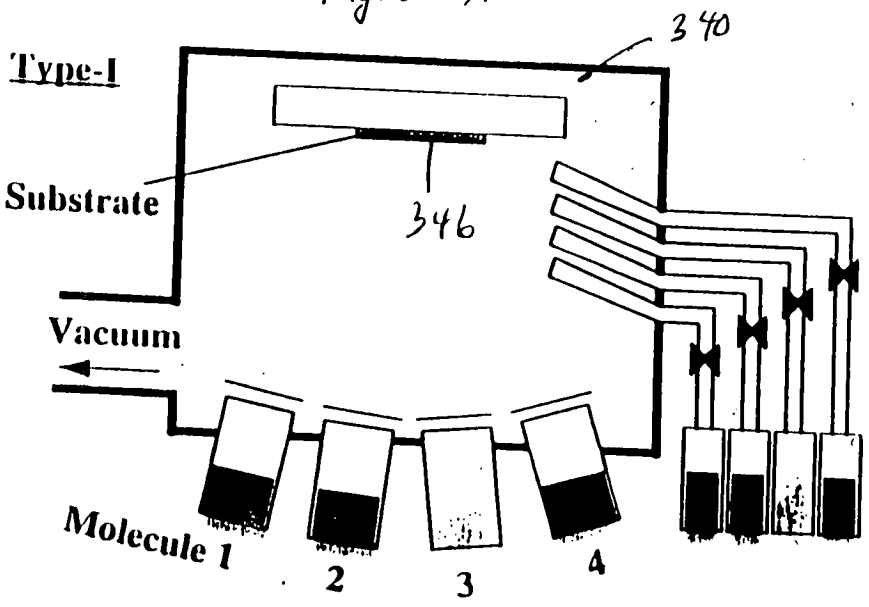


Fig 84B

Fig. 85A



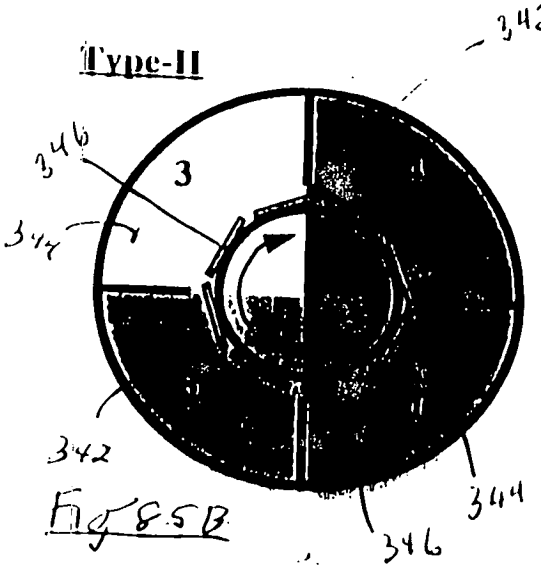
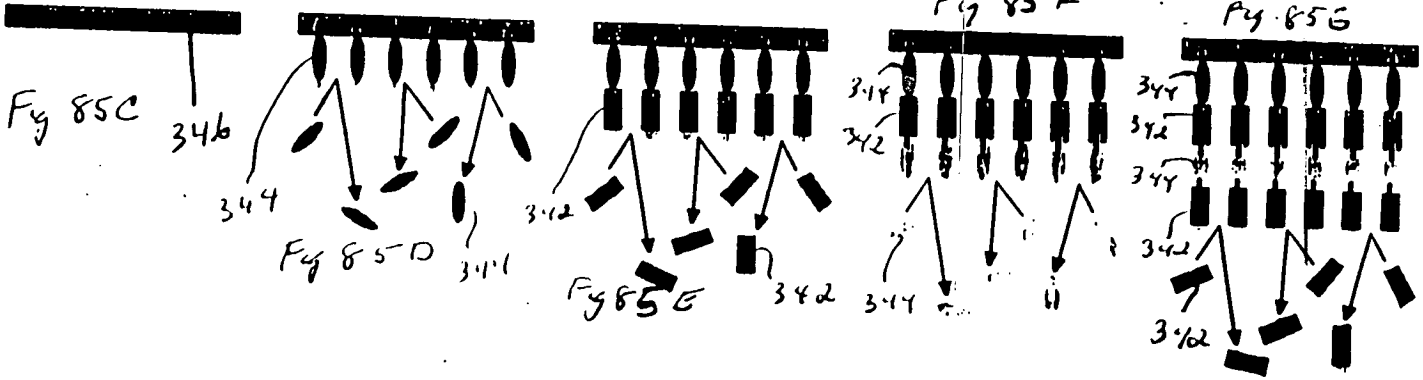


Fig 85B



Vapor Phase Deposition Vs. Spin coating

	Spin coating	Vapor Phase Deposition	
		CVD	MLD
-Coverage Controllability	Low	High	High
-Thickness Accuracy/Uniformity	Low	Medium	High
-Deposition Rate	High	Medium	Low
-Molecular-level Controllability	Low	Medium	High
-Selective Deposition	No	Yes	Yes
Selective Molecular Alignment	No	Yes	Yes

(High & Yes are preferable)

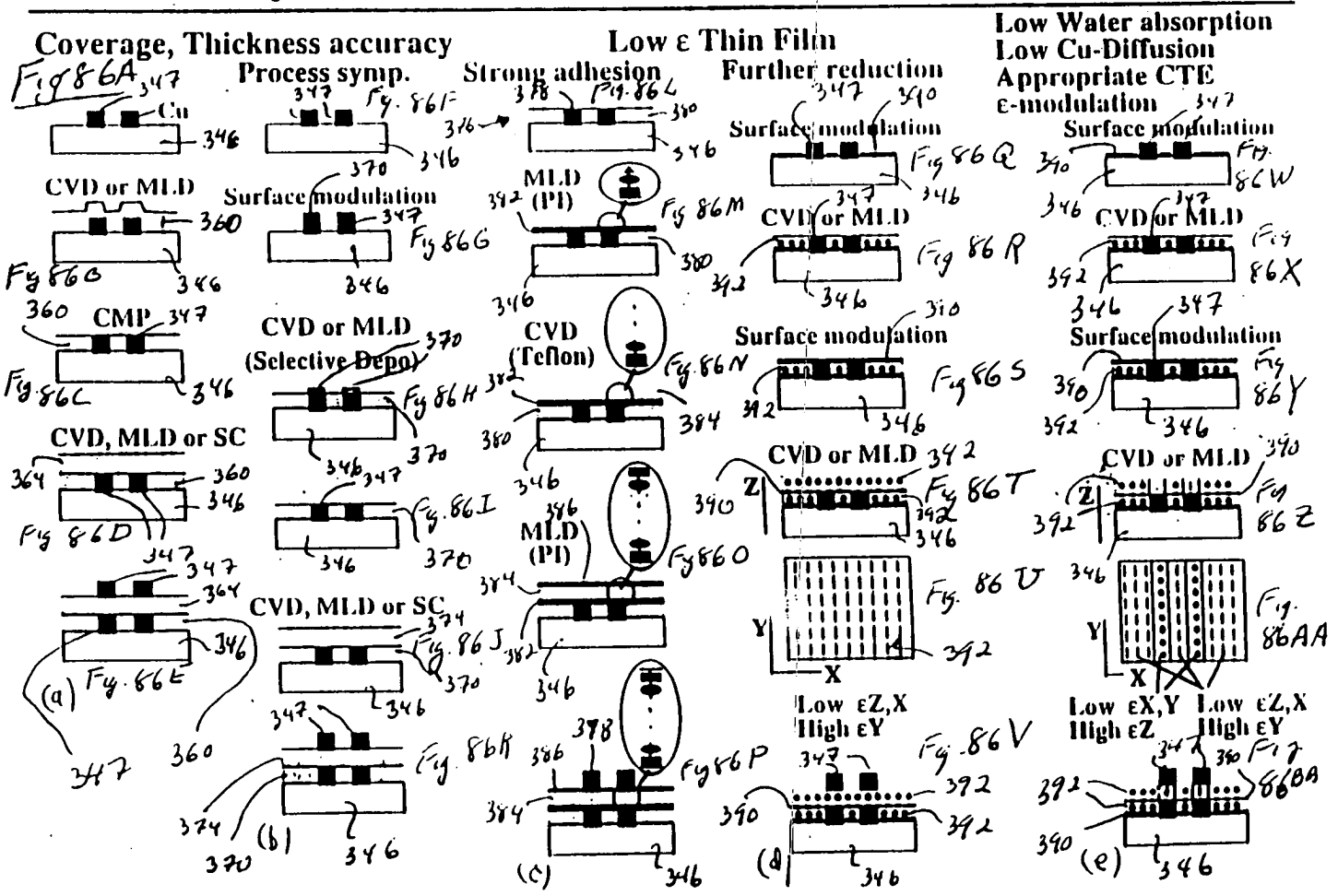
Fig 8514

-Conformable coverage and Thickness accuracy/uniformity
-CVD/MLD are superior to Spin Coating

- Low ε insulator with strong adhesion
-MLD may provide high adhesion with the Molecular-Level Controllability

-Options
-CVD/MLD can do # Selective Deposition (hydrophilic/hydrophobic surface)
Selective Molecular Alignment (surface treatment)
may provide further ε reduction, process simplification, and low Cu-diffusion

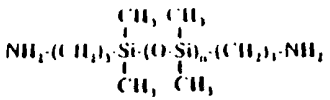
Examples of MLD & CVD application to MCM processes



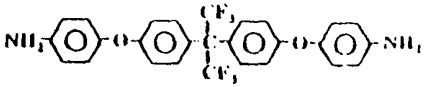
PMDA

naphthalene dianhydride (ND)

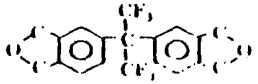
ODA



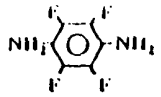
SiDA



Bis-OAF



6FDA



VT4-DA

Fig. 86CC

alkylamine-coated Si	ND ⇨ Bis-OAF⇨ ND ⇨ Bis-OAF ⇨ • • • ⇨ ND ⇨ SiDA	
Si	SiDA ⇨ 6FDA⇨	Bis-OAF+ 6FDA ⇨ SiDA
Si	SiDA ⇨ ODA ⇨ 6FDA⇨ VT4-DA ⇨ 6FDA⇨ • • • ⇨ ODA ⇨ SiDA	

1. Masking

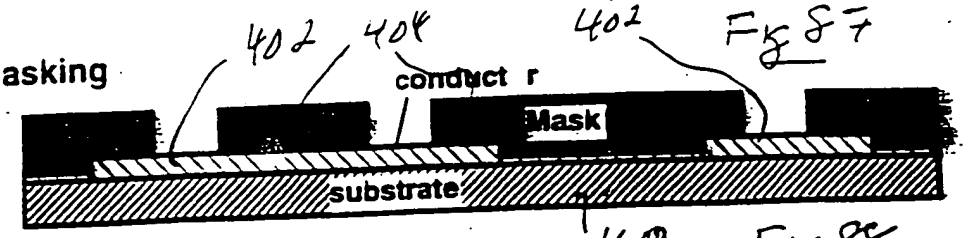


Fig 87

Fig 88

2. Electroplating Solder

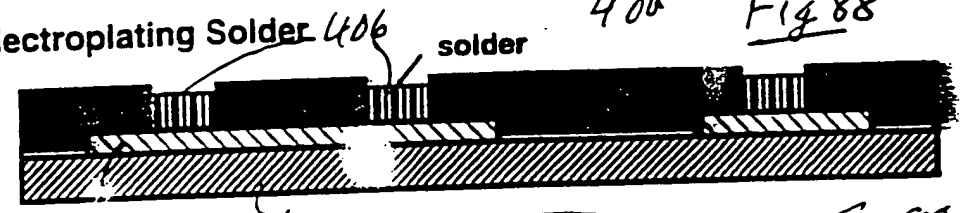


Fig 89

3. Mask Strip

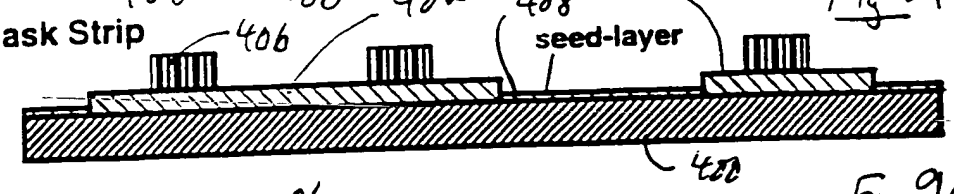


Fig 90

4. Seed Etch

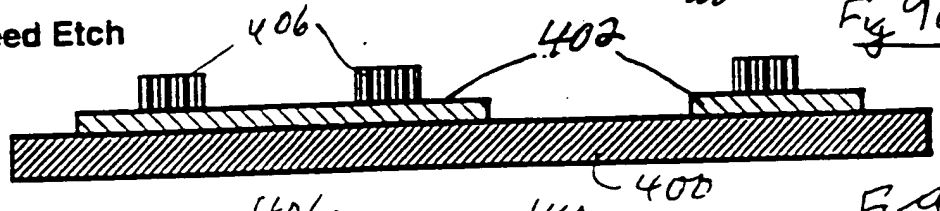


Fig 91

5. Fluxing

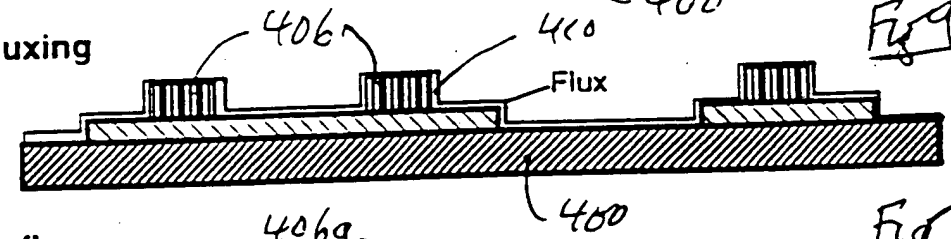


Fig 92

6. Reflow

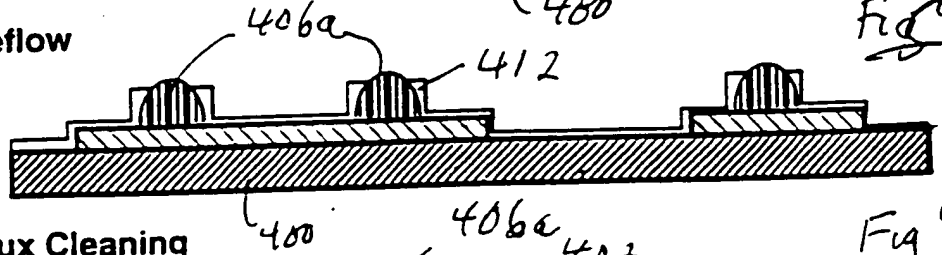
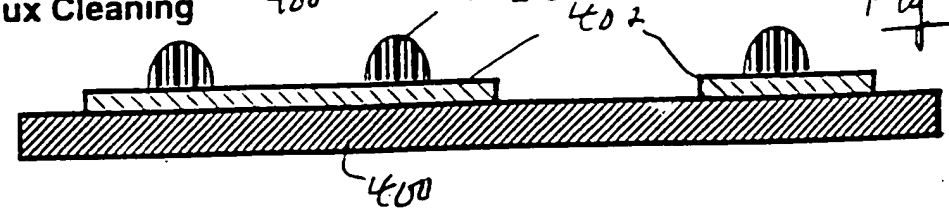


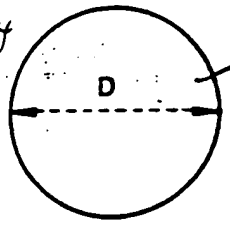
Fig 93

7. Flux Cleaning



Geometric dimensions of the electroplated bumps.

Fig 94



Top view

406

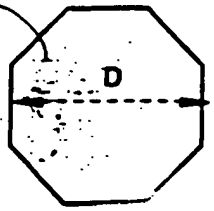
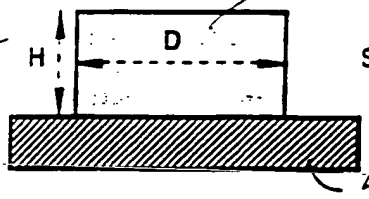


Fig 95

Fig 96

406



Side view

406

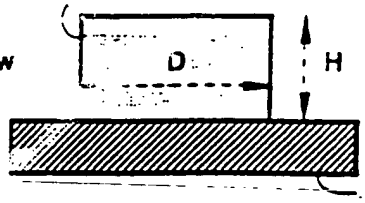
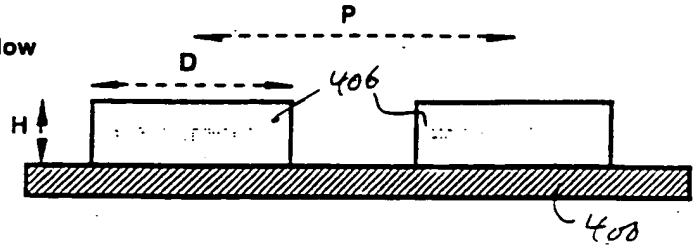


Fig 97

Geometric shape change of electroplated solder bumps by reflow process

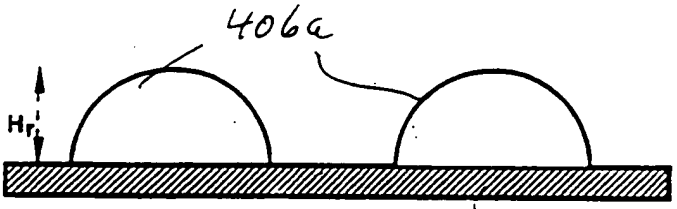
Before Reflow

Fig 98



After Reflow

Fig 99



Schematic drawing of bridged bumps

Bridged Bumps

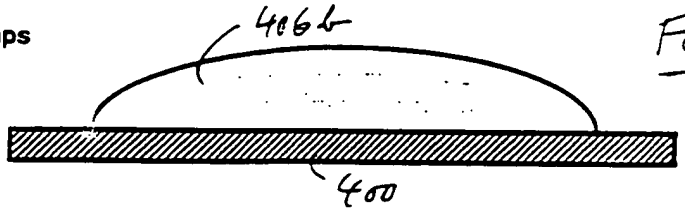


Fig 100

Direct Plating Process

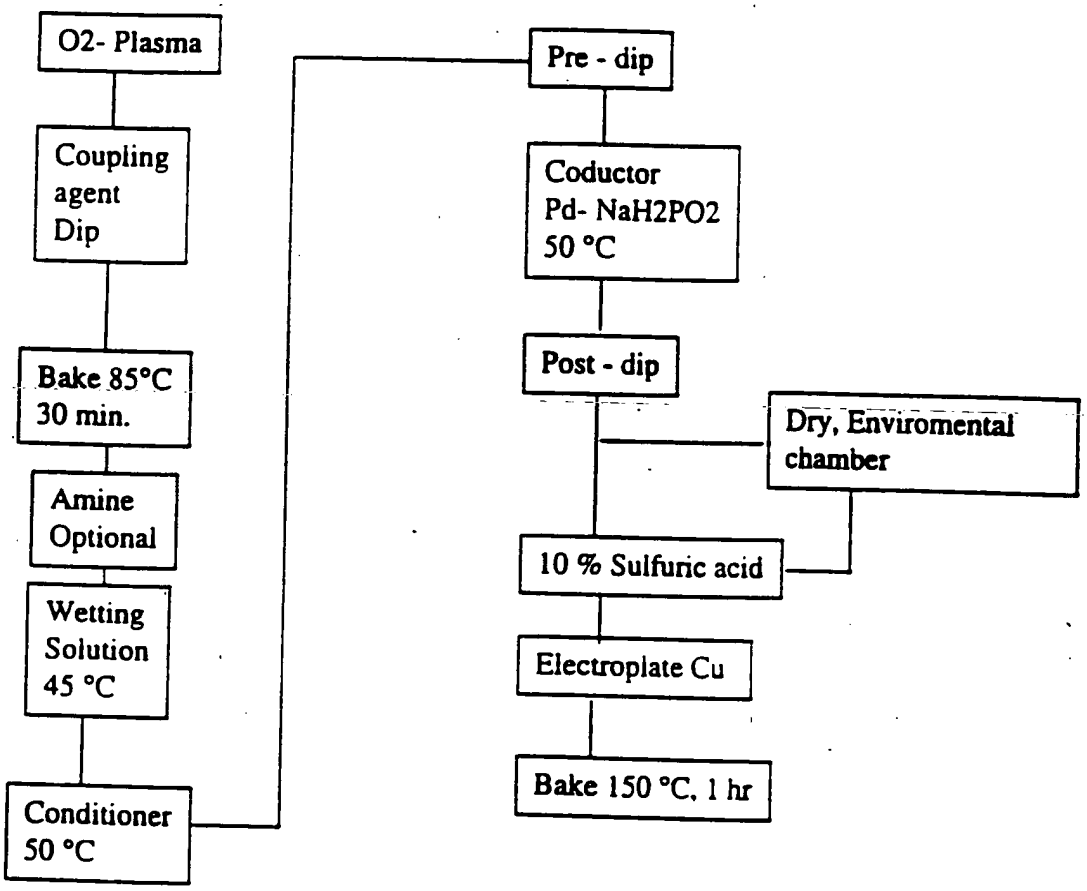
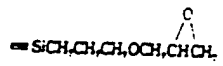
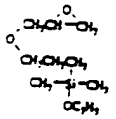


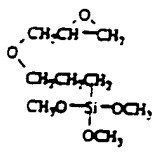
Fig 101A

Fig 10/B

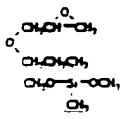




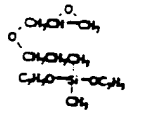
(3-GLYCIDOXYPROPYL)DIMETHYLETHOXY-SILANE
$C_{10}H_{22}O_3Si$



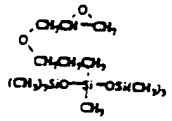
(3- GLYCIDOXYPROPYL)TRIMETHOXYSILANE
3-(2,3-EPOXYPROPOXY)PROPYLTRIMETHOXYSILANE
$C_9H_{20}O_5Si$



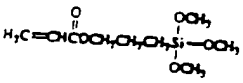
(3-GLYCIDOXYPROPYL)METHYLDIMETHOXY-SILANE
$C_9H_{20}O_4Si$



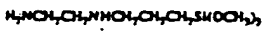
(3-GLYCIDOXYPROPYL)METHYLDIETHOXY-SILANE
$C_{11}H_{24}O_4Si$



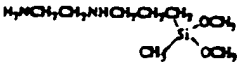
(3-GLYCIDOXYPROPYL)BIS(TRIMETHYL-SILOXY)METHYLSILANE
$C_{13}H_{32}O_4Si_3$



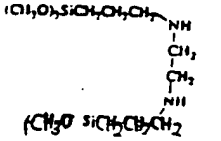
(3-ACRYLOXYPROPYL)TRIMETHOXY-SILANE, 95%
$C_9H_{18}O_5Si$



N-(2-AMINOETHYL)-3-AMINOPROPYLTRI-METHOXYSILANE
$C_8H_{22}N_2O_3Si$



N-(2-AMINOETHYL)-3-AMINOPROPYLMETHYL-DIMETHOXYSILANE
$C_8H_{22}N_2O_2Si$



BIS[3-TRIMETHOXYSILYL)PROPYL]-ETHYLENEDIAMINE.
$C_{14}H_{36}N_2O_6Si_2$

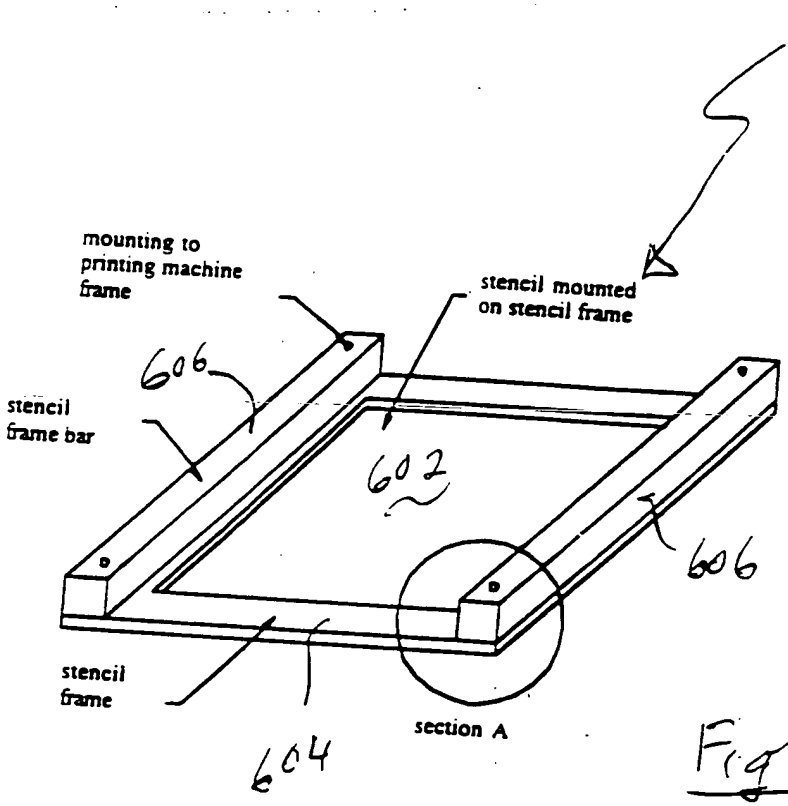


Fig 102

Stencil Frame Layout.

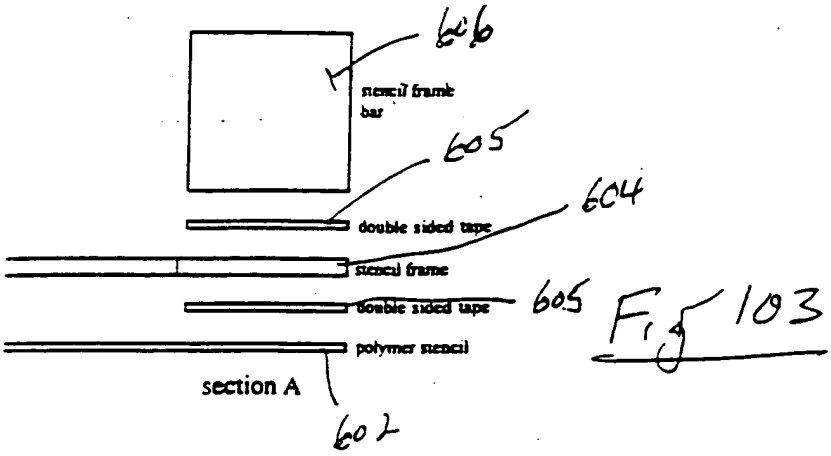


Fig 103

Section View of Stencil Frame Components.

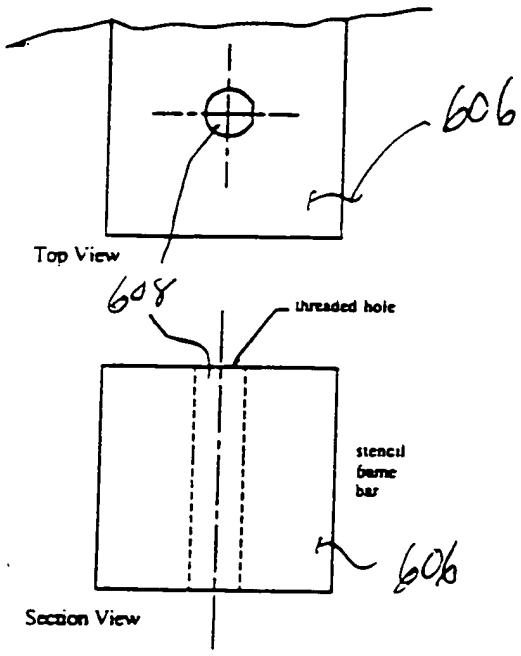
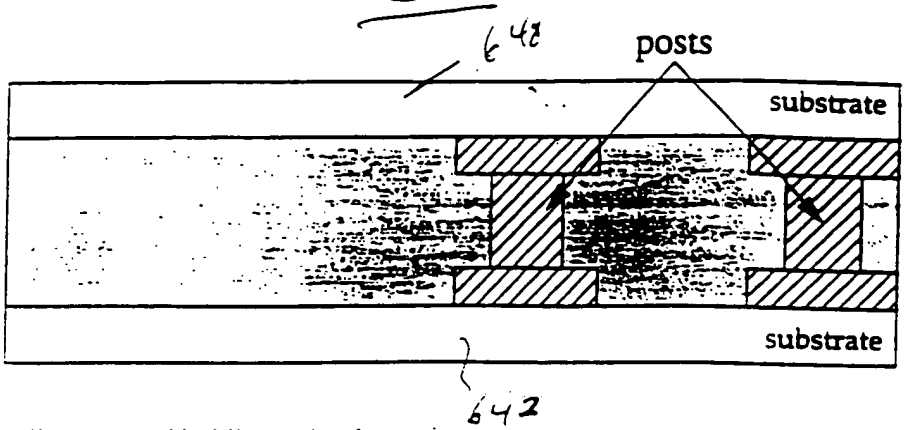


Fig 104

Tapped Hole in Stencil Frame Bar.

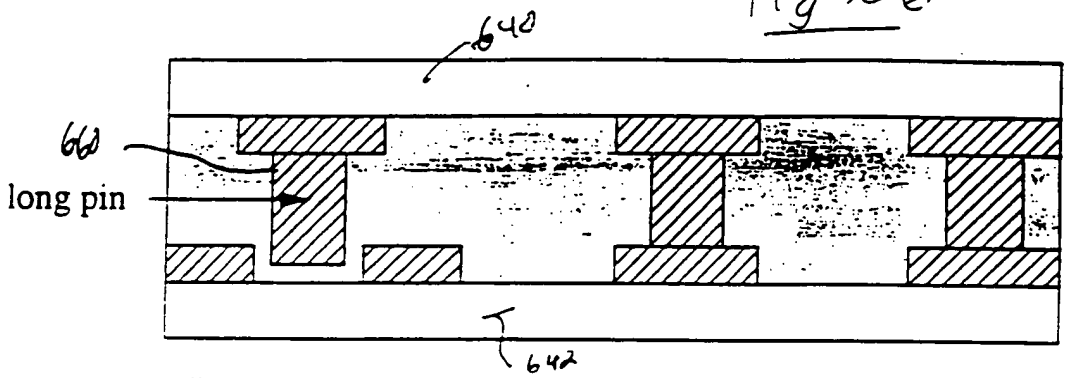
Traditional joining

Fig 105



Alignment and holding using long pin

Fig 106



Alignment and holding using thick pads

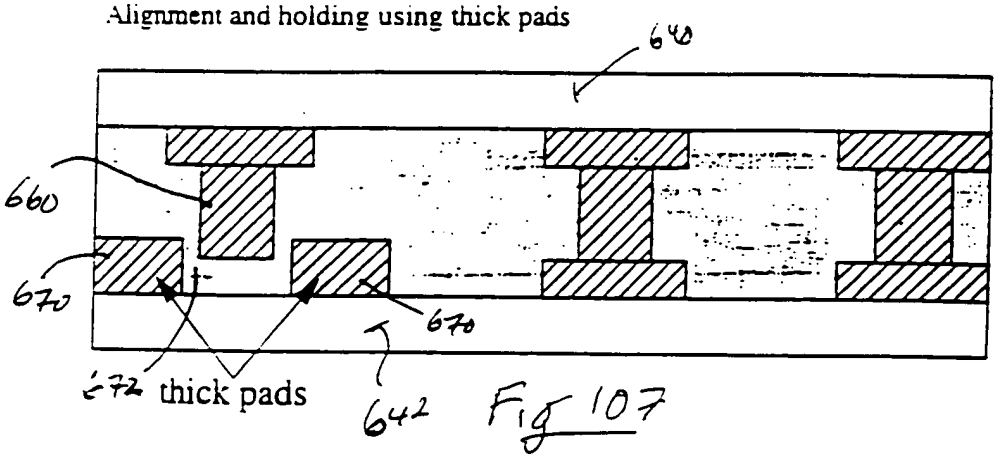


Fig 107

Build-up process for long pin

Fig 108

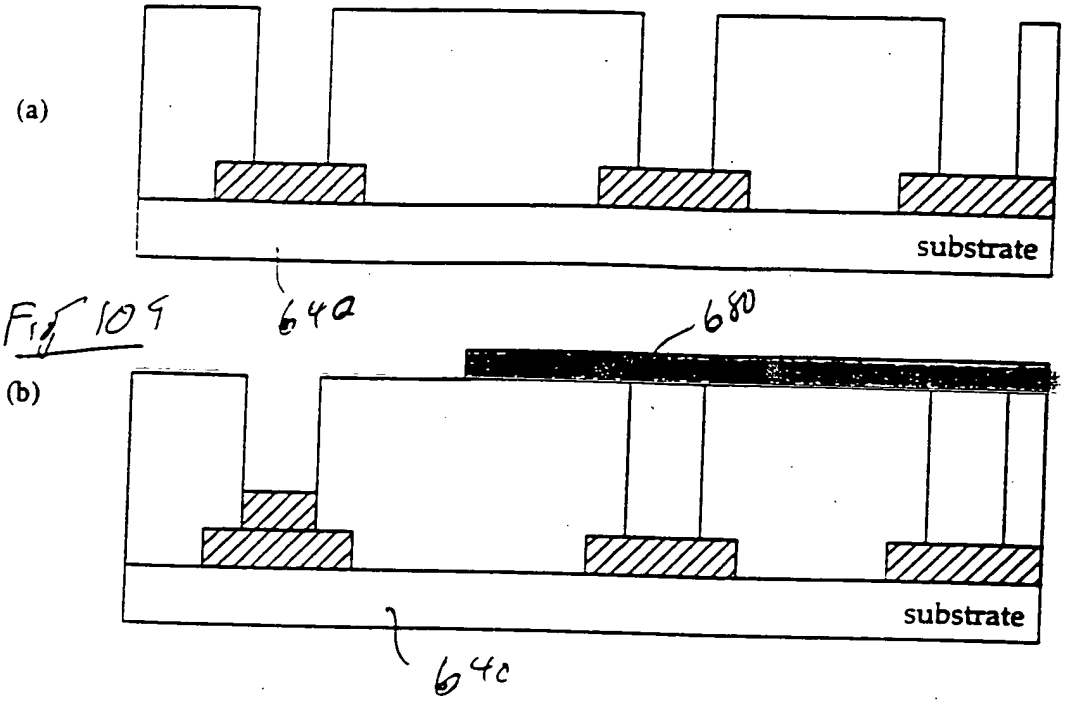


Fig 110

Fig 111

Another build-up process for long pin

(a)

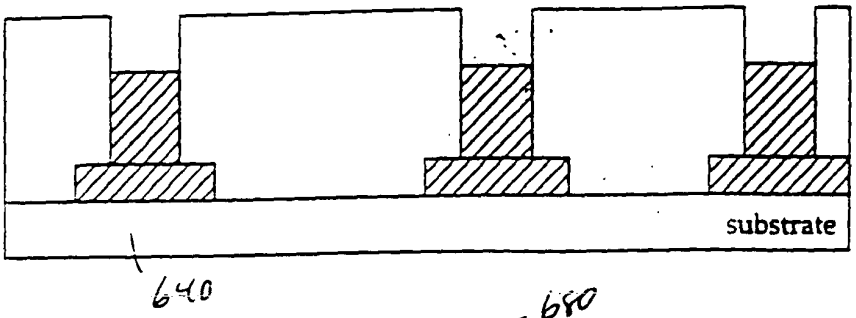


Fig 112

(b)

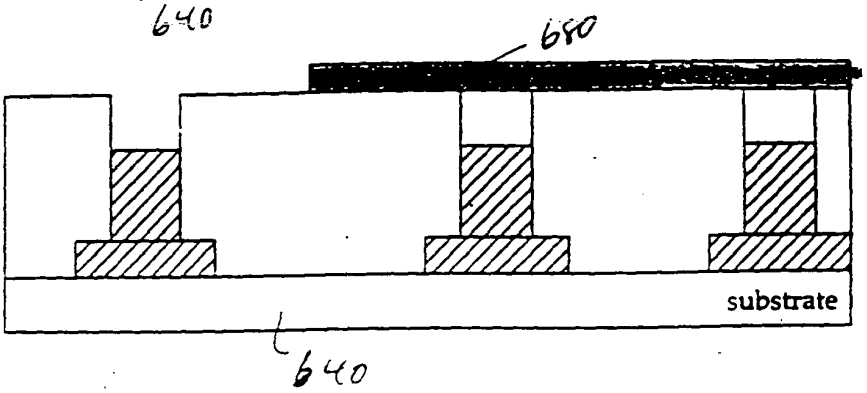
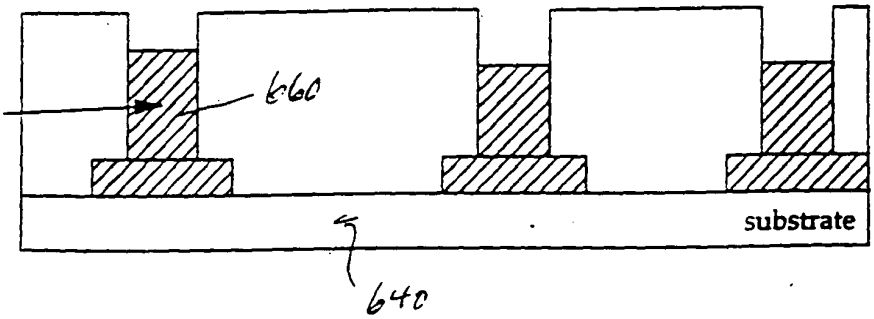
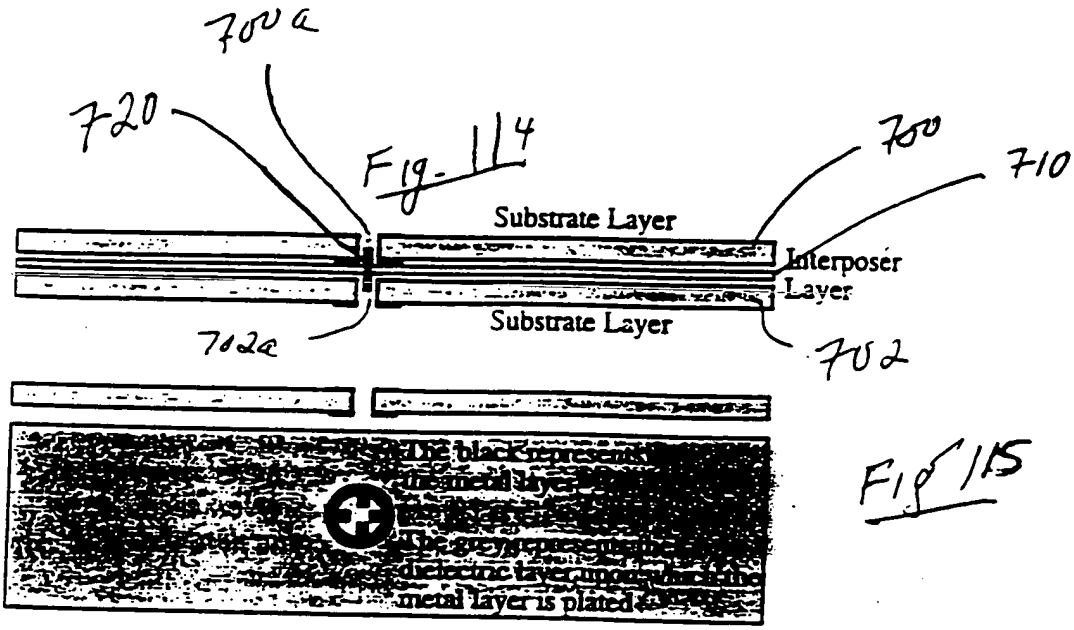


Fig 113

(c)




700a
720
Fig. 114
700
710
Substrate Layer
Interposer
Layer
Substrate Layer
702a
702
Fig 115

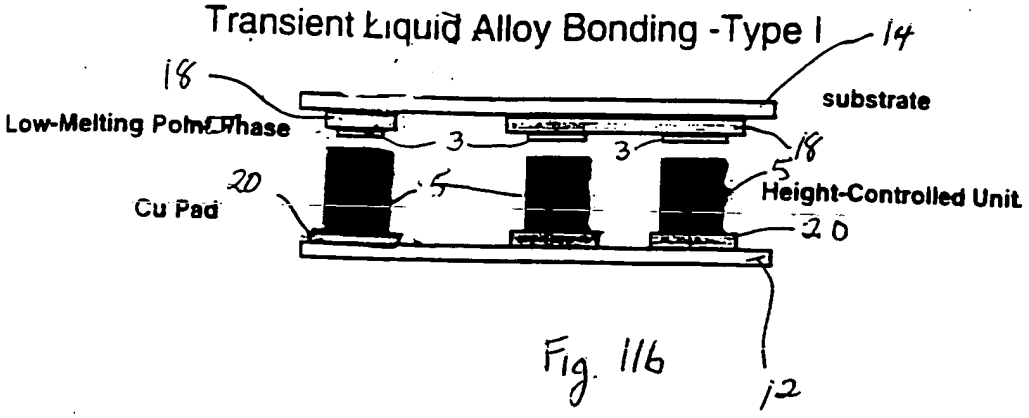


Fig. 116

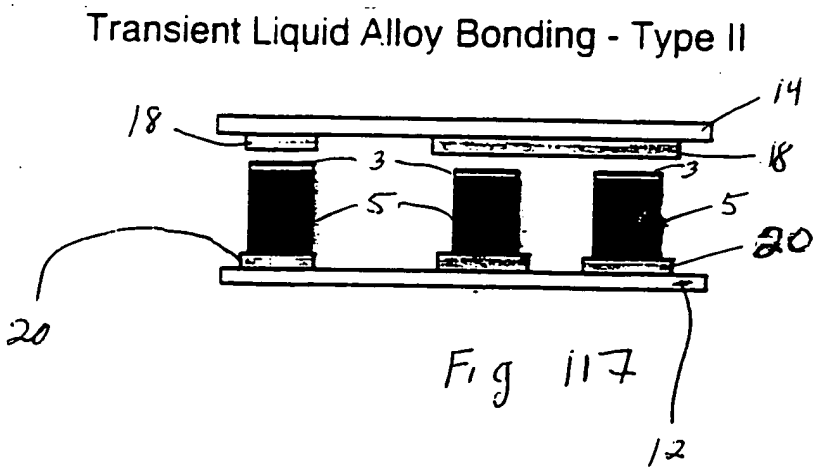


Fig 117

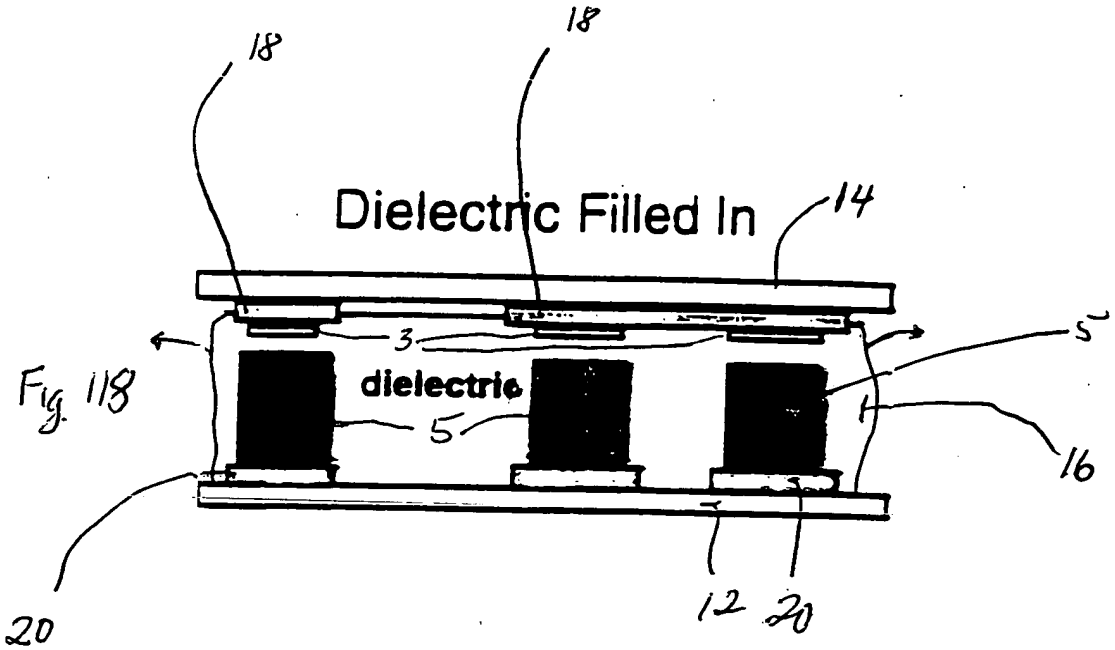


Fig 118

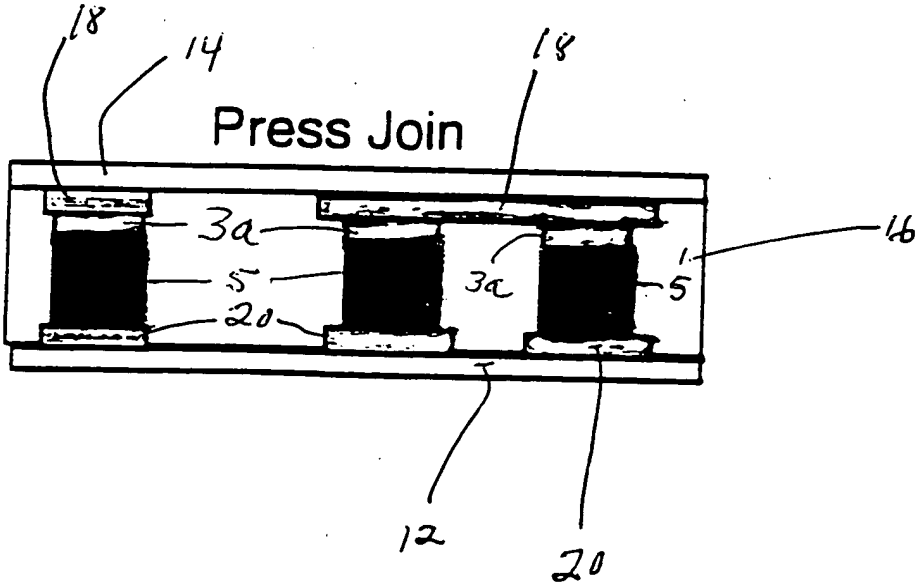


Fig 119

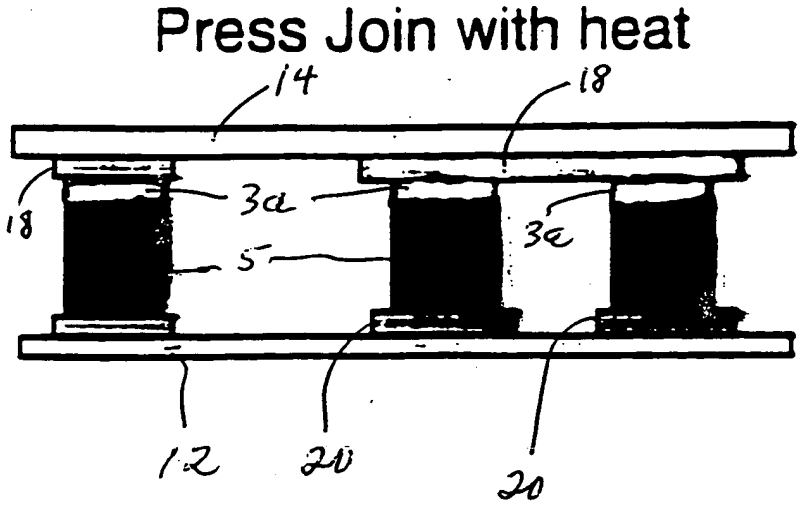


Fig 120

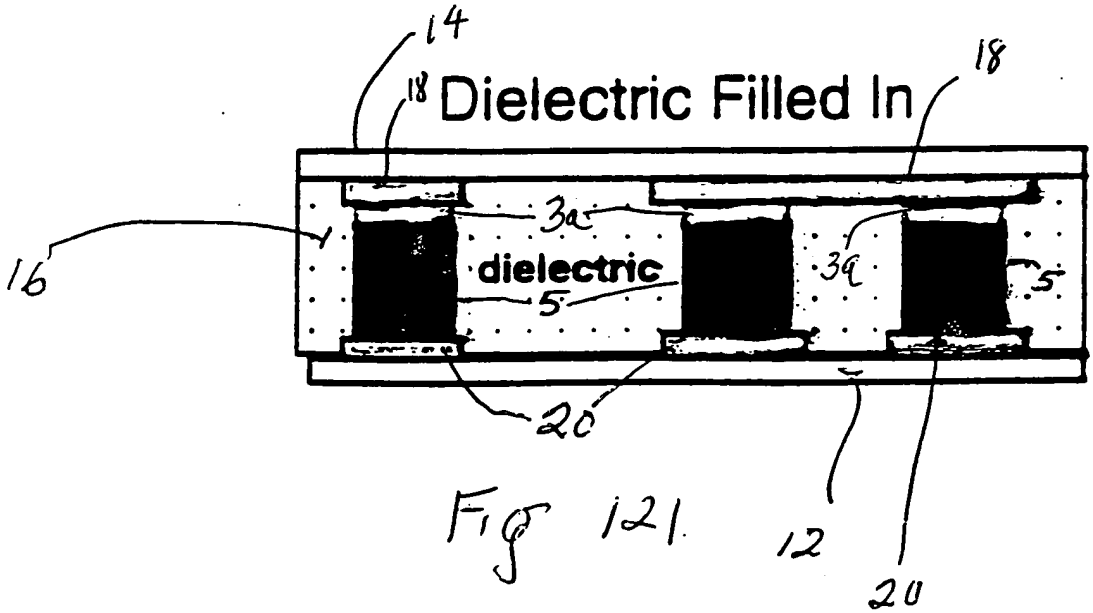


Fig 121

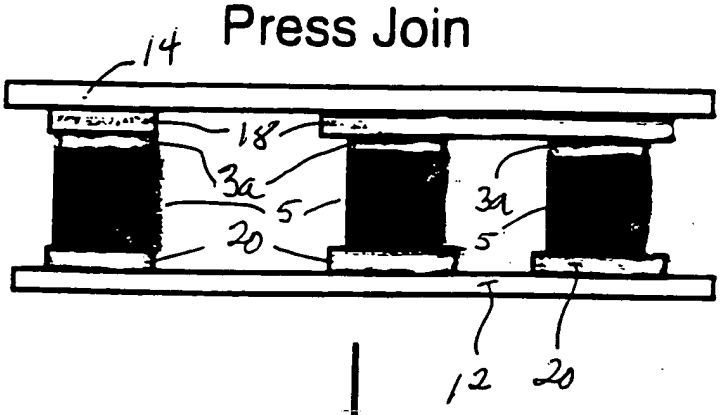


Fig 122.

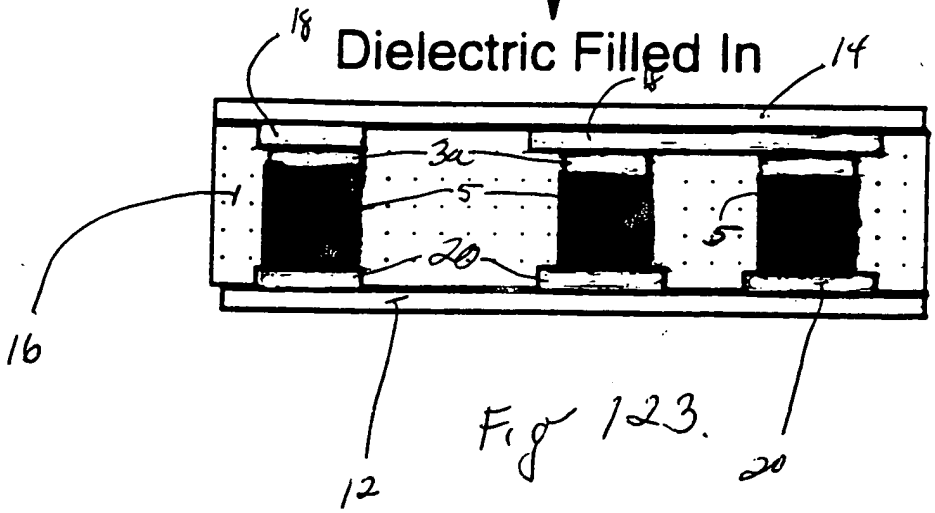


Fig 123.

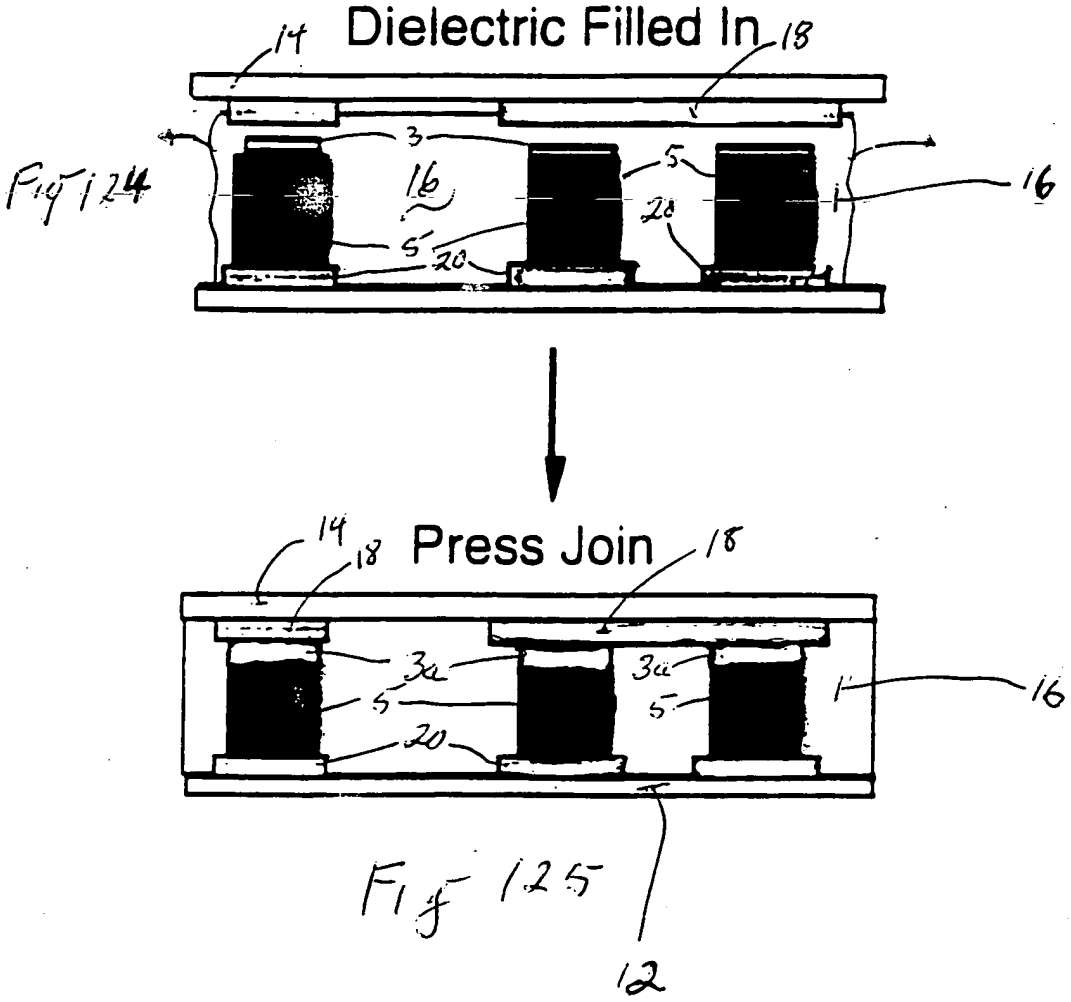


Fig 124

Fig 125